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ION IMPLANTED GaAs I.C. PROCESS TECHNOLOGY

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for period 12/01/77 through 02/28/78

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Principal Investigator

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The investigation of a new method of growing semi-insulating GaAs, aimed at minimizing silicon contamination, has been initiated during this quarter. An increase in the yield of semi-insulating material, which passes qualification tests, was observed during the last month of the quarter.

Data are presented for silicon implanted GaAs with doses varying from  $1.7 \times 10^{13}$  ions/cm<sup>2</sup> to  $1.7 \times 10^{15}$  ions/cm<sup>2</sup> with annealing temperatures ranging from 800 to 900°C. Electron concentrations as high as  $2 \times 10^{18}$  cm<sup>-3</sup> were obtained.

The uniformity of photolithography results has been studied by determining the variation in length of nominal 1  $\mu$ m long FETs gates over an IC wafer. The standard deviation was found to be only 0.15  $\mu$ m. Initial experiments to evaluate the possibility of stepping and repeating a 3 x 3 array, rather than the present 2 x 2 array have been carried out. The 1  $\mu$ m lines were adequately defined over the 3 x 3 array. These high quality photolithography results are promising for the extension of the GaAs IC process to LSI complexity.

The system for automatic device characterization (capitalized with Rockwell funds) is now capable of acquiring and displaying diode I-V characteristics measured on an automated probe station. The software for measuring, recording, and analyzing FET characteristics is at an advanced state of development.

Measurements of the performance of NOR gates and ring oscillators have been carried out as a function of operating temperature. The transfer characteristics of NOR gates were measured for temperatures up to 103°C, and showed insignificant variations with temperature. Ring oscillator performance was measured from 25 to 100°C. Only a slight decrease in oscillation frequency was observed over this temperature range. These results indicate that GaAs ICs should be capable of operation at temperatures as high as those for silicon integrated circuits.

A simple analytical model of GaAs MESFETS has been developed at Cornell University to calculate various MESFET parameters. The results agree well with those of a more complicated computer analysis for a 1  $\mu$ m gate GaAs MESFET.

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FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Science Center as the prime contractor with two universities and a crystal growth company as subcontractors. The effort is sponsored by the Materials Science Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. The Rockwell program manager is Fred A. Blum. The principal investigators for each organization are:

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## TECHNICAL SUMMARY

This report covers the third quarter of a GaAs integrated circuit (IC) program. The purpose is to develop an ion implanted planar process technology for GaAs ICs with the goal of developing LSI capability in a short period of time. The fabrication approach is based on multiple localized implantations directly into the semi-insulating GaAs substrate to form device areas insulated by the unimplanted regions of the substrate. A new circuit concept involving a combination of Schottky diodes and depletion mode Schottky barrier FETs, is being employed to form logic gates capable of high speed and very low power operation.

This program requires a research effort on all the multiple facets of the process development. The research activities range from substrate fabrication and ion implantation technology to design, fabrication and evaluation of test circuits. These activities are carried out by the Science Center with the support of three subcontractors, Caltech, Cornell and Crystal Specialties, Inc.

The following is a summary of the accomplishments of the program in the third quarter. Details will be found in the following sections of the report.

1. Bulk Crystal Growth (Sec. 2.1). Crystal Specialties has continued supplying all the qualified semi-insulating substrate material



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required by the program. The yield of material qualified for ion implantation was 32%, lower than the first quarter yield, but higher than the second quarter yield, and peaking significantly during the final month of the quarter. A new growth method aimed at minimizing Si contamination, has been implemented, and the results are now under evaluation.

## 2. Evaluation of Alternate Sources of Semi-Insulating GaAs

(Sec 2.2). A slight modification in the capping technique for the qualification tests was made, so that the process is now identical to the process for actual IC fabrication. The change consists of using a thin  $\text{Si}_3\text{N}_4$  layer with a  $\text{SiO}_2$  overcoat instead of a single thick  $\text{Si}_3\text{N}_4$  dielectric cap. Samples from Morgan Semiconductors and Sumitomo Electric were evaluated. One out of three Morgan samples qualified. The Sumitomo material has not yet successfully passed the qualification test.

## 3. Gettering of Semi-Insulating Substrates (Sec. 2.3). Gettering experiments on substrates which did pass the qualification tests have been initiated. The object of those tests is to determine whether or not gettering treatments can improve the properties of doped layers. No conclusive evidence of gettering effects has been found to date.

## 4. Ion Implantation (Sec 3.1). The study of doping of GaAs by Si implantation has been continued at Cal Tech. Good activation (>70%) was observed for samples implanted with doses as high as $1.7 \times 10^{14} \text{cm}^{-2}$ and annealed at $850^\circ\text{C}$ or higher. The carrier concentration increases very





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slowly with the dose, but carrier concentrations as high as  $2 \times 10^{18} \text{cm}^{-3}$  have been obtained.

5. Device and Circuit Fabrication (Sec. 3.2). Initial evaluation of the possibility of using larger wafers for IC fabrication with the projection mask aligner stepping and repeating a 3x3 array (2.1x2.1cm) rather than the present 2x2 array has been carried out in order to evaluate the quality of the photolithography. The results have been encouraging, and they indicate that it is reasonable to proceed to actual test fabrication using large wafers. A system for the plasma deposition of  $\text{Si}_3\text{N}_4$  as a dielectric between first and second layer metalization is now operational.

A demonstration of the capability of the projection mask aligner was made by measuring the length (nominally  $1 \mu\text{m}$ ) of 132 FET gates uniformly distributed over a wafer. A mean value of  $1.01 \mu\text{m}$  was determined with a standard deviation of 15%. Such excellent accuracy and uniformity meet the goal of developing a manufacturable planar GaAs process.

6. Automatic Measurement System (Sec. 4.1). Significant progress has been made in the construction of an automatic measurement system capable of stepping over a wafer and automatically measuring and analyzing device characteristics. The basic measurement system is operational, and the software is at an advanced stage of development. At the end of the reporting period, it was possible to record diode I-V characteristics, and the software for measuring, recording, and analyzing FET data was being developed.



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7. Temperature Dependence of IC Operation (Sec. 4.3). Excellent behavior of the circuit dc characteristics at temperatures as high as  $133^{\circ}\text{C}$  has been demonstrated. It has been shown using appropriate test patterns designed on the mask that the isolation between closely spaced contacts ( $3\mu\text{m}$  gap) provided by the unimplanted substrate is well above the tolerance level of  $10^7\Omega/\square$  even at  $133^{\circ}\text{C}$ . The I-V characteristics of test FET devices and the transfer-characteristics of NOR gates showed insignificant variations. Ring oscillators were also evaluated over a 25 to  $100^{\circ}\text{C}$  range. The oscillation frequency decreased slightly as the temperature was increased when the bias conditions were optimized for maximum speed.

8. Switching Speed Analysis (Sec. 4.4). A simple analytical model has been used at Cornell University to calculate the saturation current, channel conductance, transconductance, charge under the gate, gate-to-source and drain-to-gate capacitances, cut-off frequency, characteristic switching time, and power delay product of GaAs MESFETs. The results have been verified by comparison with a two-dimensional computer calculation. They also agree well with the results of the computer analysis and with experimental data for  $1\mu\text{m}$  gate GaAs MESFETs.



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## 1.0 INTRODUCTION

The objective of this program is the development of a planar, ion implanted integrated circuit process technology for GaAs in order to take advantage of the superior electrical properties of GaAs which make possible high speed, low power digital integrated circuits. The results of ring oscillator tests which were carried out in the second quarter of this program clearly demonstrate that the expected short propagation delays and low dynamic switching energies can indeed be achieved in depletion-mode GaAs integrated circuits. This demonstration is an important milestone in the first phase of the program which is 17 months in length. The goal at the end of the first phase is the demonstration of the ability to fabricate planar circuits of MSI complexity. This program requires efforts in a number of different areas ranging from the growth and evaluation of semi-insulating GaAs to the design and testing of demonstration circuits. The bulk of the work is carried out at the Rockwell International Science Center. However, significant assistance is provided by three subcontractors, Crystal Specialties, Inc., California Institute of Technology, and Cornell University.

An important aspect of the work during the past quarter was the measurement of the characteristics of test devices and circuits as a function of operating temperature. Excellent behavior of dc circuit characteristics at temperatures as high as 133°C was demonstrated. It was shown, using appropriate test patterns included on the mask, that the isolation between closely spaced contacts (3μm gap) provided by the unimplanted substrate is well above a tolerance level of  $10^7 \Omega/\text{cm}$  even at 133°C. The I-V



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characteristics of test FET devices and the transfer characteristics of NOR gates showed insignificant variations. Ring oscillators were also evaluated over a 25 to 100°C range. The oscillation frequency decreased only slightly as the temperature was increased when the bias conditions were optimized for maximum speed. The results of these measurements of device and circuit performance as a function of operating temperature are quite encouraging, and indicate that GaAs integrated circuits should be capable of operation at temperatures as high as those at which Si integrated circuits are functional.

Significant results in a number of other areas are also contained in this third quarterly report. A new method of growing semi-insulating GaAs is being evaluated at Crystal Specialties, Inc. There was a significant increase in the yield of qualified semi-insulating material tested during the last month of the third quarter. The study of silicon implantation has been continued and a more complete characterization of silicon as an implanted dopant has been achieved.

A number of experiments related to process evaluation or improvements have been carried out. These include determination of the doping profiles of IC active layers, and the study of the variation of the length of 1µm gates over an IC wafer. Initial evaluation of the possibility of stepping and repeating a 3x3 array with the projection mask aligner rather than the present 2x2 array has been carried out. Evaluation of silicon nitride films from a recently purchased plasma nitride deposition system has been initiated.



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Substantial progress has been made on the automation of data acquisition on the Electroglas probe station which is used for low frequency measurement of various test devices and circuits. At the end of the quarter, it was possible to automatically measure and record diode I-V characteristics, and the software for measuring, recording and analyzing FET data was under development.

A simple analytical model of GaAs MESFETs has been used at Cornell University to calculate various MESFET characteristics. The results have been found to agree well with values obtained from a two-dimensional computer calculation and with experimental data from  $1\mu\text{m}$  gate GaAs MESFETs.



## 2.0 MATERIAL

In this section of the report, the work at Crystal Specialties on the growth of semi-insulating GaAs is discussed. Results of qualification tests during the third quarter of the program are listed, and a summary of qualification results during the second and third quarters is presented. Finally some preliminary results on the effects of gettering treatment on implantation profiles in qualified semi-insulating substrates are presented.

### 2.1 Bulk Growth of Semi-Insulating GaAs - (Crystal Specialties)

The single crystal growth of GaAs at Crystal Specialties, Inc. is progressing steadily. Problems still affect the yield and quality of microwave substrate materials, but an understanding of these problems is slowly evolving.

A high yield of electrically compensated single crystals (number of compensated crystals/number of successfully grown single crystals) is obtained without any sign of yield deterioration as in the past periods. The major problem still existing is "thermal conversion." Since silicon contamination is a possible cause of "thermal conversion" problems, a new growth method aimed at minimizing Si contamination is being evaluated. The new approach stems from the idea that in the current growth system, silicon is incorporated during the reaction period while the arsenic temperature is below 600°C. After reaction, the of the temperature arsenic reservoir is raised to 950°C, and the residual Ga<sub>2</sub>O<sub>3</sub> in the system dissociates supplying oxygen to the vapor, thus stopping the dissociation of SiO<sub>2</sub>. The new



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method consists of trying to reduce Si contamination during the reaction period by placing a capillary tube between the gallium in the boat and the arsenic in the arsenic reservoir, and adding  $\text{Ga}_2\text{O}_3$  to the gallium side of the capillary tube. As the arsenic furnace is heated, the arsenic streaming through the capillary prevents the  $\text{Ga}_2\text{O}_3$  from subliming from the gallium melt chamber into the cool ( $600^\circ\text{C}$ ) arsenic reservoir. By using this method of reaction the oxygen supplied by the dissociating  $\text{Ga}_2\text{O}_3$  is available to suppress the dissociation of the  $\text{SiO}_2$  boat and ampoule. Crystals have been grown with the new system and they are being evaluated.

Another problem under investigation is the observation of some inclusions in the substrates after polishing. These inclusions are found not only at the back of the ingot where they would be more common, but they are also observed in slices throughout the ingot. Work to identify these defects by x-ray analysis in the SEM (Sec. 2.2) is in progress. On the assumption that the inclusions might be SiC particles coming from the grit used to sandblast the quartz boat, cleaning procedures have been improved by including ultrasonic rinsing, but this has failed to totally eliminate this problem. Other grits such as  $\text{SiO}_2$ , BN and  $\text{Al}_2\text{O}_3$  are being evaluated. A factor that adds interest to this problem is the possibility that SiC inclusions might be an additional source of contamination, with some bearing on the thermal conversion problem.

During this reporting period, the single crystal yield (number of single crystals/number of growth runs) was 60%. The compensation yield (number of electrically compensated crystals/number of single crystals) was 94%. The yield of crystals qualified for implantation (number of qualified



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crystals/number of electrically compensated single crystals) was 32%. Although the percent of crystals which did not convert (qualified for implantation) over this quarter is lower than during the first quarter, there was a significant increase in the yield of qualified material during the final month of the quarter. This increase in yield may be associated with increased experience with growth in the new ( $\langle 110 \rangle$ ) crystalline direction, and with decrease in the time required to react the elemental gallium and arsenic.

## 2.2 Evaluation of Alternate Sources of Semi-insulating GaAs (Science Center)

During the third quarter, samples were received from Crystal Specialties, Morgan Semiconductors and Sumitomo Electric. Chromium doped wafers were not available during this period from Laser Diode Inc. All wafers were evaluated using the procedure and specifications outlined in Quarterly Technical Report No. 1, Section 3.1. A modification was made in the cap qualification tests in order to be consistent with the integrated circuit process. In the qualification test and the IC process the cap now consists of  $\sim 1100\text{\AA}$  of reactively sputtered silicon nitride overlaid with  $\sim 2000\text{\AA}$  of silicon dioxide.

The physical properties of wafers received during this period were similar to those of the last quarter. A general improvement in wafer flatness has been observed from all suppliers with the best performance from Crystal Specialties. Table 2.2-1 indicates the flatness of some recent lots of GaAs as determined with a non-contact, laser interferometer. The values quoted represent variations over a normal size wafer measured over a 2 inch distance





in the long dimension. A 21x21mm process area (3x3 array) would typically show a flatness variation of about  $\pm 1.5\mu\text{m}$ . Crystalline defects were observed from selected wafers taken from lots 3602, 3473, & 3475. Some examples of these defects are shown in Fig. 2.2-1. Optical microscopy indicates the presence of gallium inclusions and chromium precipitates. Analytical measurements will be made upon these samples using x-ray analysis during the next quarter.

Analytical methods to study the properties of semi-insulating GaAs which is rejected during the qualification procedure are currently being investigated. A highly sensitive TSC (Thermally Stimulated Current) apparatus will be used to measure the rejected semi-insulating samples. This TSC method has shown a sensitivity of  $10^{11}$ - $10^{12}\text{cm}^{-3}$  for mid gap states in  $\text{BaTiO}_2$ . Recent work on photoconductivity in Cr doped GaAs has also given useful results. It is planned to further explore the use of this technique.

Table 2.2-2 contains a summary of electrical qualification results during this period. The overall fraction of electrically qualified material has increased in comparison to the second quarter, but still is less than 50%. A summary of the substrate qualification results for the second and third quarters of the program is shown in Table 2.2-3. Figure 2.2-2 illustrating the fraction qualified per month shows an encouraging trend. February was a record month in which 67% of the material received qualified for processing.

### 2.3 Gettering (Science Center)

Gettering experiments designed to investigate the effects of various gettering treatments on implantation results in qualified substrate material have been initiated. Results have been obtained from a few samples so far.



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TABLE 2.2-1  
GaAs SUBSTRATE FLATNESS  
(As Received)

Vendor	Ingot No.	Flatness
Crystal Specialties, Inc.	XS 3473	$\pm 4\mu\text{m}$
	XS 3474	$\pm 3\mu\text{m}$
	XS 3475	$\pm 2\mu\text{m}$
	XS 3602	$\pm 4\mu\text{m}$
	XS 3552	$\pm 2\mu\text{m}$
	XS 3608	$\pm 5\mu\text{m}$
	XS 3716	$\pm 4\mu\text{m}$
	XS 3756	$\pm 2\mu\text{m}$
	XS 3737	$\pm 2\mu\text{m}$
Mitsubishi-Monsanto Co.	G101-36F	$\pm 4\mu\text{m}$



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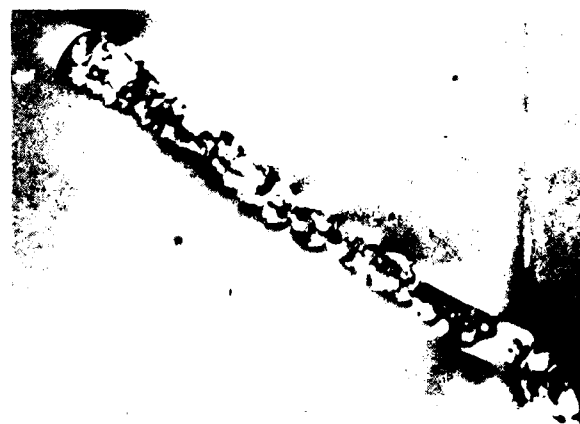
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XS 3473



XS 3602



XS 3602

280X

Fig. 2.2-1 Defects observed in chromium doped GaAs substrates.



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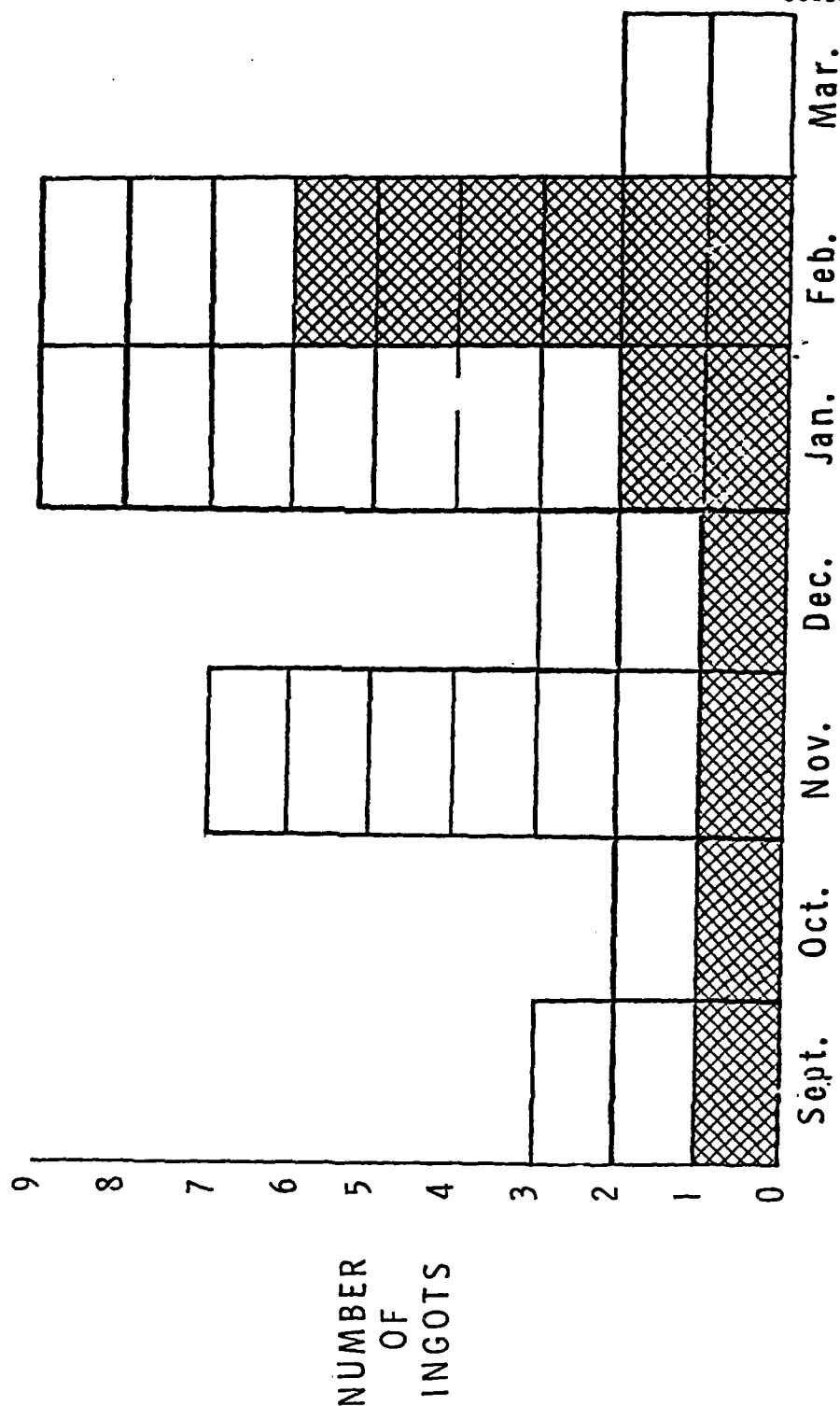


Fig. 2.2-2 GaAs ingots received vs. qualified, second period 9/77 - 3/78.



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TABLE 2.2-2  
SUBSTRATE QUALIFICATION FOR ION IMPLANTATION  
SHEET RESISTANCE ( $\Omega/\square$ )

Supplier	Front Kr	Back Kr	Growth Orientation*
<u>Crystal Specialties, Inc.</u>			
3712	$10^4$	$10^3$	<111>
3716	$10^7$	$10^7$ Qualified	
3717	$10^3$	$10^7$	
3725	$10^3$	$10^4$	
3736	$10^2$	$10^3$	
3737	$10^7$	$10^7$ Qualified	
3744	$10^3$	$10^7$	
3753	$10^3$	$10^5$	
3756	$10^7$	$10^6$ Qualified	
3757	$10^7$	$10^7$	In Progress
3774			
3779	$10^3$	$10^6$	
3786	$10^4$	$10^5$	
3787	$10^6$	$10^5$	
3801	$10^8$	$10^7$ Qualified	
3802	$10^7$	$10^6$ Qualified	
3803	$10^5$	$10^7$	
3805	$10^8$	$10^7$ Qualified	
3806	$10^4$	$10^7$	
3809	$10^7$	$10^7$ Qualified	
3557	$10^7$	$10^7$ Qualified	
3396	Control	$10^6$	



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TABLE 2.2-2 (Cont'd)

Supplier	Front Kr	Back Kr	Growth Orientation*
<u>Sumitomo Electric Ltd</u>			
M0047-1		5x10 <sup>4</sup>	
<u>Morgan Semiconductor Inc.</u>			
MSI 11-1	6x10 <sup>5</sup>	9x10 <sup>5</sup>	
MSI 5-26	3x10 <sup>6</sup>		
MSI 9-79	10 <sup>4</sup>	10 <sup>5</sup>	<111>
MSI 7-5	10 <sup>6</sup>	5x10 <sup>6</sup> Qualified	<111>

\* <110> except where noted.



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TABLE 2.2-3

GaAs SUBSTRATE SUMMARY  
9/77 - 3/78

Contractors	Total Ingots Tested	Total Ingots Qualified	Percent Qualification
1. Crystal Specialties, Inc.	35	12	34%
2. Morgan Semiconductor, Inc.	7	1	14%
3. Sumitomo Electric, Ltd.	3	0	0%
4. Mitsubishi-Monsanto Co.	2	1	50%*

\* Note the small number of boules sampled



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The data for material which was treated by impact sound stressing or by laser scribing of the back surface (this was carried out with the cooperation of Dr. G.H. Schwuttke of IBM, East Fishkill Laboratory) indicated that these treatments do not result in any significant change in Se doping profiles. Preliminary data have also been obtained for ion bombardment. The gettering treatment involved bombardment with 400 keV K ions to a dose of  $1 \times 10^{15}$  ions/cm<sup>2</sup> at room temperature. The bombarded wafers were coated with silicon nitride on both sides and annealed at 850°C for 30 min. Following removal of the Si<sub>3</sub>N<sub>4</sub> cap, approximately 1 μm of GaAs was removed from the bombarded surface by chemical etching. Selenium implantation profiles have been measured in such gettered material and in ungettered, controlled wafers taken from the same slice of semi-insulating GaAs. The results show a significant difference in the implantation profiles. However, this data should not be taken as a conclusive indication of gettering effects due to the limited number of samples measured. A much larger number of samples are being processed and results for them will be reported in the next quarter.





### 3.0 PROCESS DEVELOPMENT

Further data on Si implantation in GaAs have been obtained during this quarter. The results show that Si implantation at room temperature can be used to produce electron concentrations greater than  $1 \times 10^{18} \text{cm}^{-3}$  utilizing an  $850^{\circ}\text{C}$  anneal temperature. The fabrication effort has been concentrated on the evaluation of the photolithography and on activation of a new plasma silicon nitride deposition system. Results are presented on the variation in length of  $1 \mu\text{m}$  gates and on the possibility of stepping a  $3 \times 3$  array rather than the present  $2 \times 2$  array. Preliminary results on operation of the plasma nitride system are presented.

#### 3.1 Silicon Implantation in GaAs (Caltech and Science Center)

The dependence of the ratio of the sheet electron concentration to the implantation dose ( $N_S/N_D$ ) on the anneal temperature ( $T$ ) with  $N_D$  as a parameter is shown in Fig. 3.1-1. For low doses,  $N_S/N_D$  is found to approach unity. The highest electron activity of about 90% is obtained for the sample implanted with  $N_D = 1.7 \times 10^{13} \text{cm}^{-2}$  and annealed at  $900^{\circ}\text{C}$  for 30 min. Samples implanted with the higher doses show considerably lower values of  $N_S/N_D$  for the same anneal temperature. The functional dependence of  $N_S/N_D$  on  $T$  follows a similar trend for all doses except for the highest one, which is quite different.

Electron concentration ( $n$ ) and mobility ( $\mu$ ) profiles are shown for three samples implanted with the same dose,  $N_D = 5.7 \times 10^{13} \text{cm}^{-2}$  and annealed at three different temperatures in Fig. 3.1-2. The Si concentration

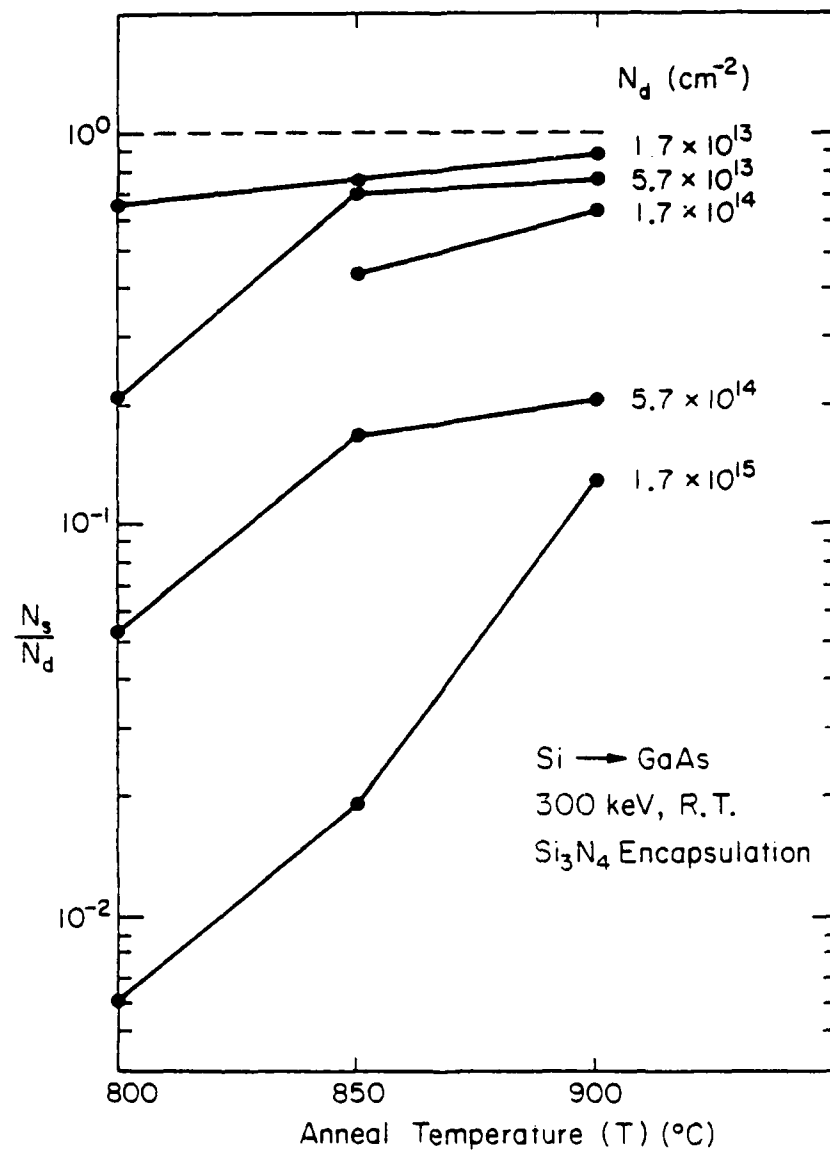


Fig. 3.1-1 Ratio of sheet electron concentration to implantation dose as a function of anneal temperature for Si implanted GaAs.



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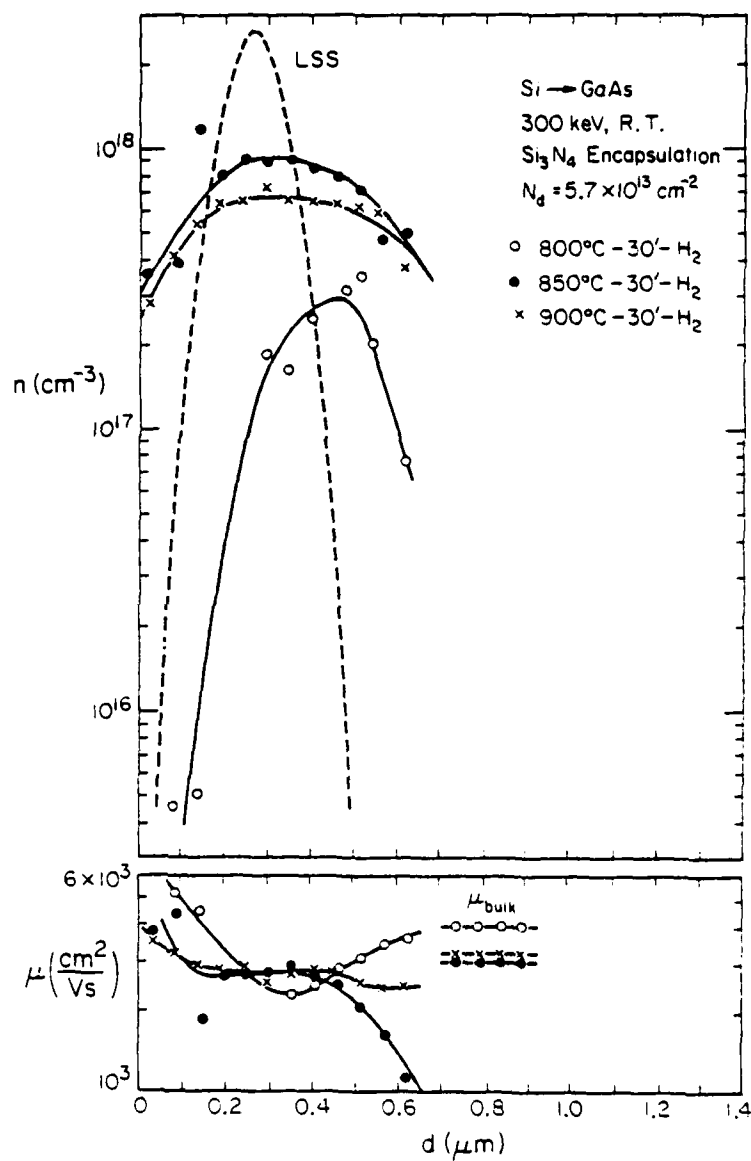


Fig. 3.1-2 Electron concentration and mobility profiles for Si implanted GaAs.



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profile calculated using LSS range parameters and a Gaussian approximation<sup>(1,2)</sup> is also plotted for comparison. For the samples annealed at 850 or 900°C the electron concentration profiles are approximately Gaussian with their maxima located at roughly the depth predicted by the LSS theory. However, the profiles are broader than predicted from the LSS range parameters. This broadening may be due to diffusion. The electron concentration profile for the sample annealed at 800°C indicates that a temperature of 800°C is not high enough to electrically activate the implanted Si. The mobility profiles for the three samples show that the absolute values of mobility are all within a factor two. The values of  $\mu$  are somewhat lower than the values of  $\mu$  in bulk GaAs<sup>(3)</sup> for electron concentrations equal to the peak values in the electron concentration profiles.

The effect of the dose  $N_d$  on the profiles of  $n$  and  $\mu$  is shown in Fig. 3.1-3, for samples which were all annealed at 850°C. It is interesting to note that, although one achieves higher values of  $n$  with higher  $N_d$ , the increase in  $n$  is much smaller than the increase in  $N_d$  (an increase in  $N_d$  by a factor of 33 produces an increase in the peak value of  $n$  by only a factor of 6). This indicates that higher values of  $N_d$  may not necessarily produce higher values of  $n$ . The mobility profiles, depicted in Fig. 3.1-3, show that the absolute value of mobility decreases systematically with increasing dose (electron concentration), a result also found in bulk GaAs.<sup>(3)</sup> However, the decrease in the mobility appears to be greater than the decrease in the bulk mobility for the same range of the peak doping concentrations.<sup>(3)</sup>



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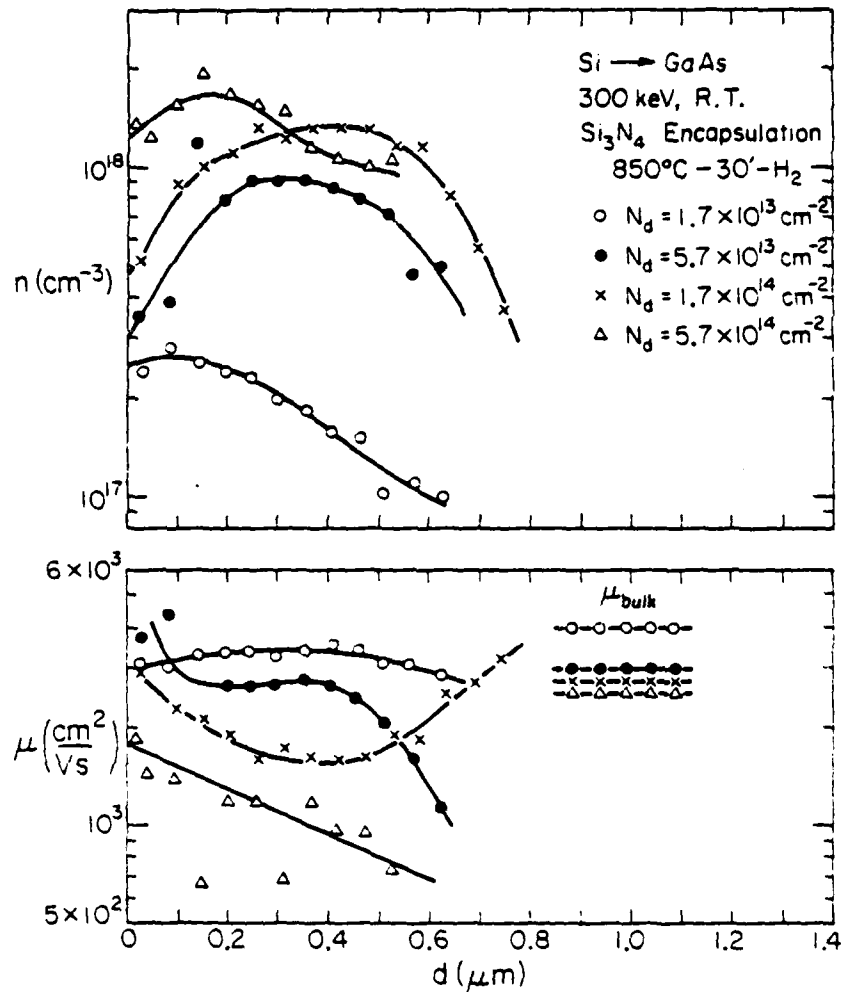


Fig. 3.1-3 Electron concentration and mobility profiles as functions of implantation dose for Si implanted GaAs.



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The different behavior of  $1.7 \times 10^{15} \text{cm}^{-2}$  implants shown in Fig. 3.1-1 is further illustrated in Fig. 3.1-4 where the profiles of  $n$  and  $\mu$  are shown for the sample annealed at  $900^\circ\text{C}$ . The carrier concentration profile is not only deep, but also flat. This result suggests that for high doses ( $10^{15} \text{cm}^{-2}$ ), the distribution of the donor ions after annealing is qualitatively different from distributions found for lower doses.

In general, from the present study of room temperature Si implants in GaAs, the following statements can be made:

- (a) For low doses ( $N_d \leq 1.7 \times 10^{14} \text{cm}^{-2}$ ) one achieves good electrical activation (50%) of the implanted Si ions when the layers are annealed at  $900^\circ\text{C}$  for 30 min in  $\text{H}_2$  with a silicon nitride cap.
- (b) Higher doses do not necessarily yield higher values of electron concentration. The highest attained doping concentration is  $2 \times 10^{18} \text{cm}^{-3}$ .
- (c) The depth profiles of the electron concentration for  $N_d \leq 5.7 \times 10^{14} \text{cm}^{-2}$  are roughly Gaussian. However, for  $N_d = 1.7 \times 10^{15} \text{cm}^{-2}$  and  $900^\circ\text{C}$  annealing, the profile is flat.
- (d) Si implantation at room temperature is a promising method of obtaining electron concentrations to about  $10^{18} \text{cm}^{-3}$ .

### 3.2 Device and Circuit Fabrication (Science Center)

Excellent progress continues to be made towards the development of an ion implanted planar GaAs process technology. At this point in the program all of the planar fabrication techniques have been demonstrated with a high degree of success.



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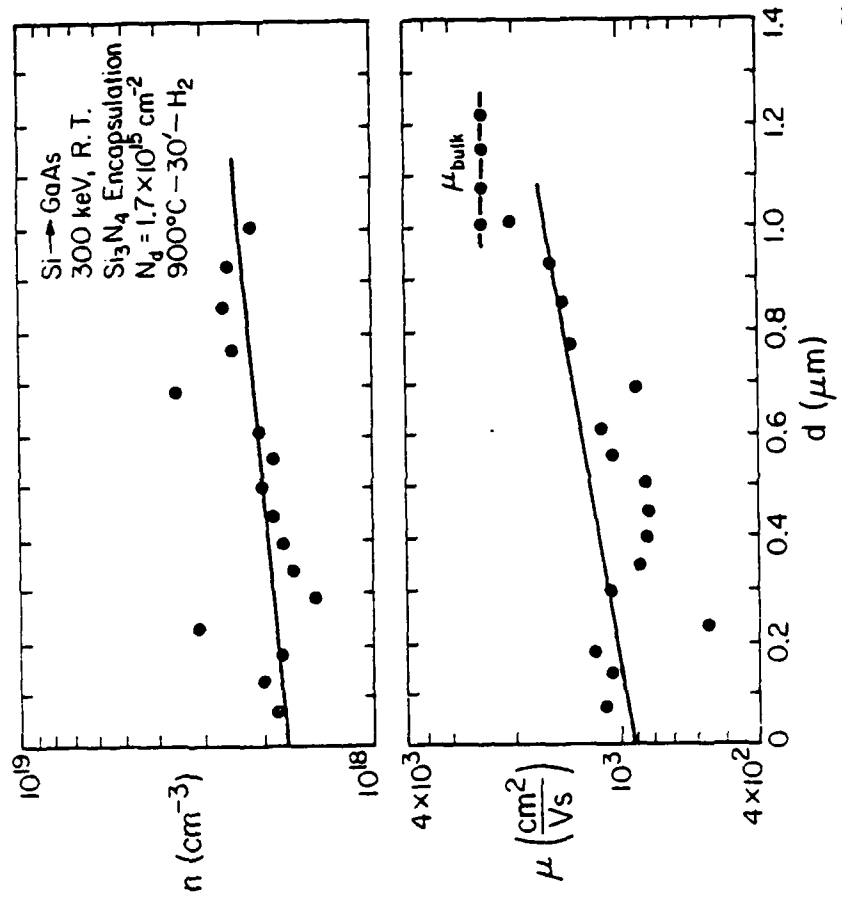


Fig. 3.1-4 Carrier concentration and mobility profiles for a Si implanted GaAs sample annealed at 900°C.



Presently, the fabrication effort is aimed at obtaining a reasonable process flow for the establishment of an initial IC data base. The purpose is to generate sufficient performance information for direct feedback into the process as well as for the identification of problem areas which will require further process development. An important part of the process feedback loop is the "on chip" active layer analysis (carrier concentration profiles) and their relationship to actual device characteristics and implantation parameters. Preliminary data on completed IC wafers will be discussed in Section 3.2.1. Section 3.2.2 will discuss the quality of the 4X projection photolithography used to fabricate GaAs ICs and the initial work on extending the stepping capability of the projection mask aligner (PMA) from 4 steps to 9 steps in order to fabricate larger wafers.

Plasma deposited  $\text{Si}_3\text{N}_4$ , currently used for the isolation between the first and second layer IC interconnects is the only fabrication capability which was not available at the Science Center at the start of this program. In Section 4.2.3 the initial evaluation of plasma deposited  $\text{Si}_3\text{N}_4$  at the Science Center and the progress made using a recently purchased apparatus are discussed.

### 3.2.1 Active Layer Analysis

In order to evaluate and monitor the active layer regions resulting from the implantation, test structures have been incorporated in the Process Monitor (PM) area of mask set AR1 for measuring the locally implanted carrier concentration profiles. (See Sec. 4.4 in the first quarterly report for a complete description of the mask set.) The multiple implantations in the





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planar process are referred to in the following manner: the FET channel selenium implant is called  $n^-$ ; the high speed Schottky diode sulfur implant is labeled  $n^+$ ; and the third optional implant for ohmic contacts is labeled  $n^{++}$ . (The  $n^{++}$  implant has not been utilized to date.) Carrier concentration profiles using capacitance-voltage (C-V) profiling techniques can be measured on the actual IC wafer test structures as well as on test chips run parallel with the IC process. Carrier concentration profiles measured on wafers fully implanted with selenium ( $n^-$ ) and sulfur ( $n^+$ ) are shown in Fig. 3.2-1. The localized implantations used in the planar process should produce areas with the same carrier concentration profiles.

Carrier concentration profiles were determined using conventional C-V techniques made on  $10^{-3}\text{cm}^2$  Schottky diode capacitors in the PM area of completed GaAs IC wafers. These profiles labeled  $n^+$  and  $n^-+n^+$  are presented in Fig. 3.2-2 along with an  $n^-$  profile measured on a chip implanted and processed in parallel with the wafer. (Parallel test chip processing is a standard process monitoring procedure.) Using a standard 1 MHz C-V profiler for measuring the  $n^-$  profile has proved inadequate because of the high sheet resistance of the  $n^-$  layer ( $\sim 2000\Omega/\square$ ). The shallower  $n^-$  profile is a result of the selenium implant, the lower  $n^+$  profile is a result of the sulfur implant while the third profile  $n^-+n^+$  is a result of both the sulfur and the selenium implant (used for ohmic contacts and for voltage level shifting diodes). As can be observed, the  $n^+$  profiles are nearly identical at a depth of  $2000\text{\AA}$  and beyond. The  $n^-+n^+$  profile differs from the  $n^+$  profile in the shallower region within  $2000\text{\AA}$  of the GaAs surface where the difference in the profiles is nearly equal to the profile of



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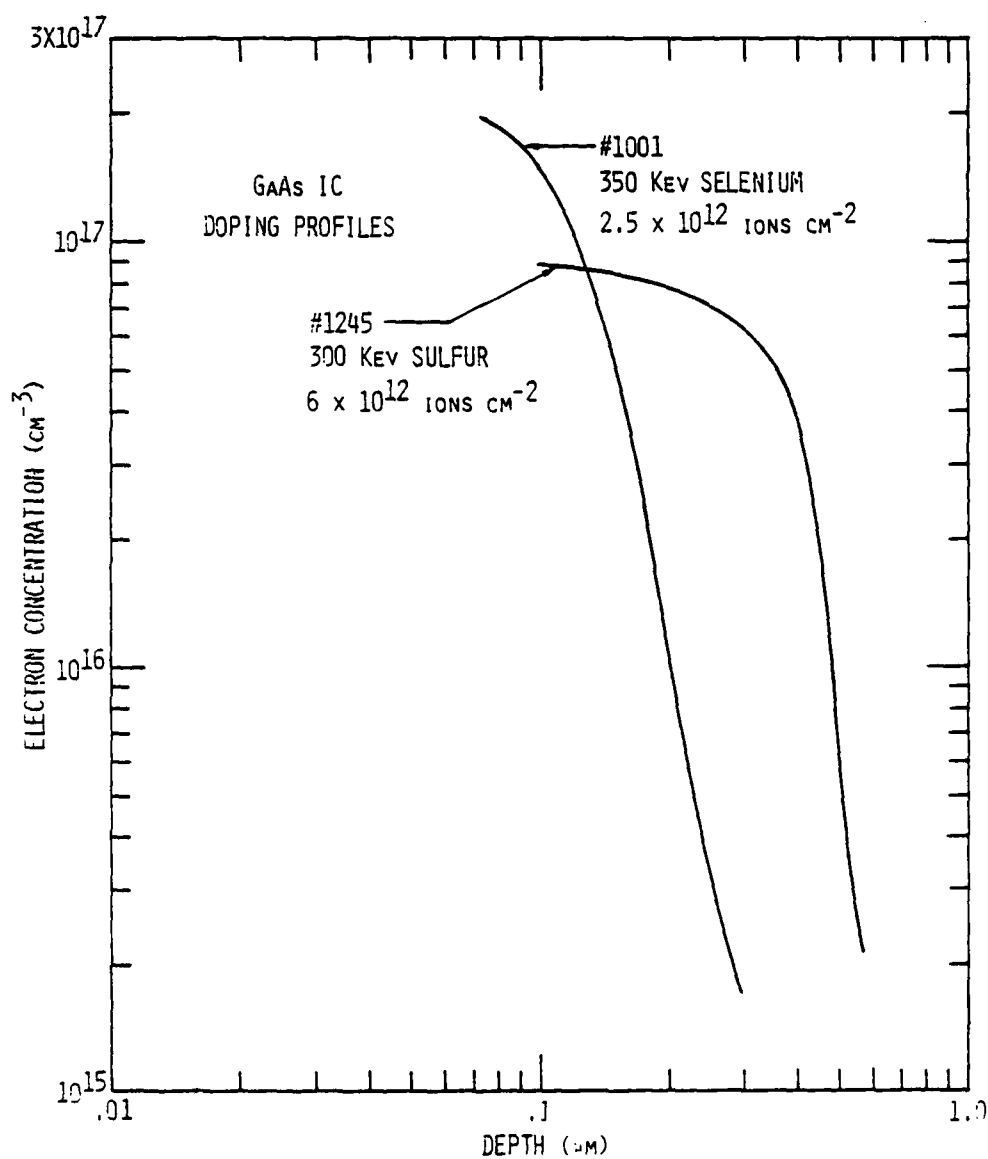


Fig. 3.2-1 Doping profiles for the FET channel selenium implant and high speed switching diode sulfur implant.



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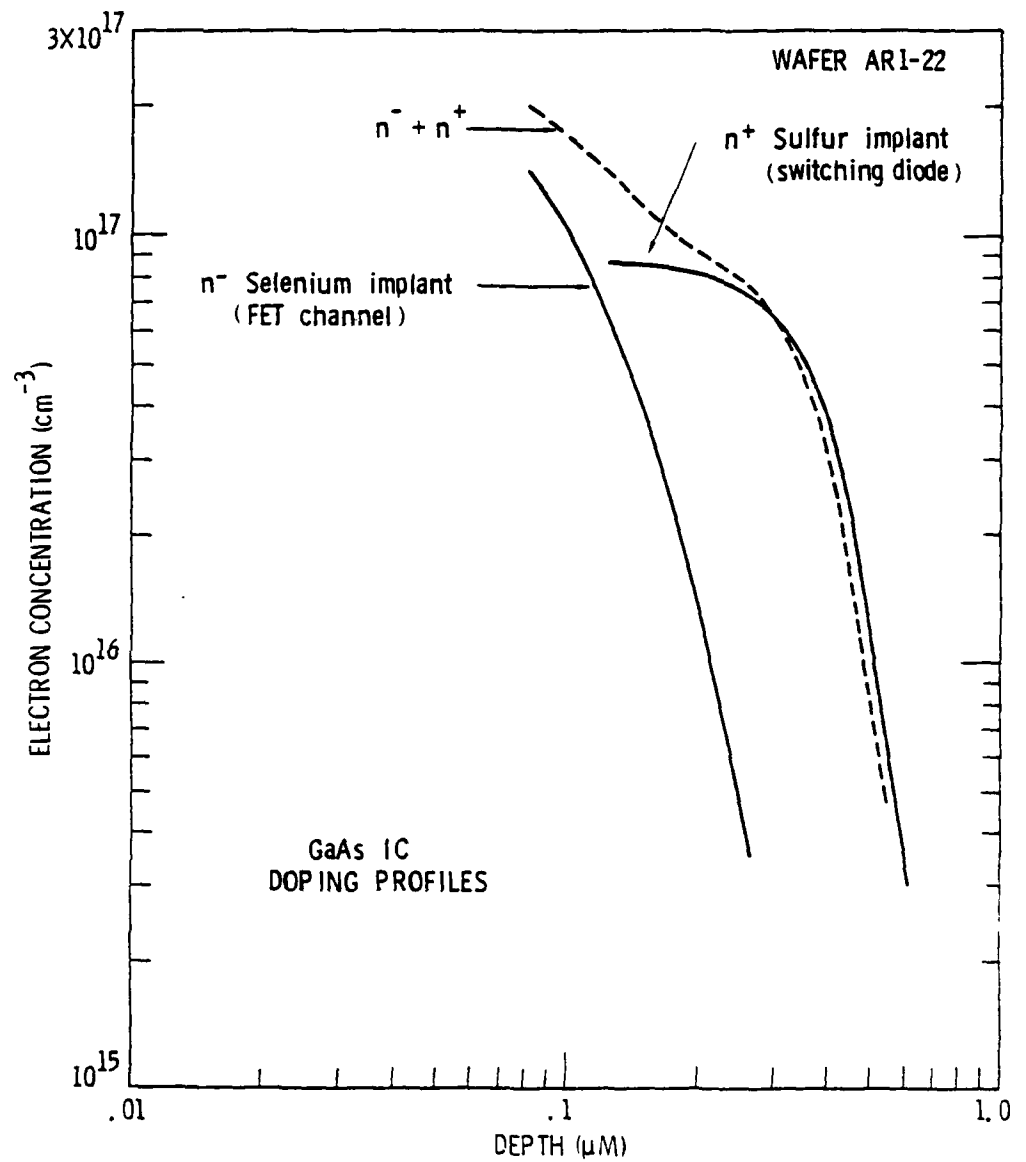


Fig. 3.2-2 Carrier concentration vs. depth profiles for the selenium  $n^-$  implant, the sulfur  $n^+$  implant, and the combined  $n^-$  selenium +  $n^+$  sulfur implant measured for IC wafer ARI-22.



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the  $n^-$  implant. The on chip IC profiles are consistent with the experimental implantation measurements presented in Fig. 3.2-1, verifying that the localized implantation results in carrier concentration profiles similar to those from the full wafer implantations. Furthermore, the additive nature of the  $n^-$  and  $n^+$  profiles has satisfied any concern relating to mixing of the selenium and sulfur implantation species in the same localized region.

### 3.2.2 Projection Photolithography

The heart of our planar GaAs IC fabrication process is the 4X projection mask aligner (PMA). Nearly all of the mask layers (minimum of six) required for the fabrication of the planar SDFL circuits contain at least some  $1\mu\text{m}$  wide lines. Such a line width requirement demands excellent resolution capability of the GaAs IC photolithographic process. It has been clearly demonstrated that the PMA can resolve  $1\mu\text{m}$  linewidths, however, it is important to determine the uniformity of linewidths across the fabricated IC wafers. In order to gather linewidth uniformly data, a GaAs IC wafer was selected at the point in the process after the Schottky gates were defined. Optical measurements were made on representative  $1\mu\text{m}$  gate metal lines with both vertical and horizontal orientation in a particular circuit containing a ring oscillator composed of nine NOR gate stages. Measurements were made on 132 gates equally distributed across the  $14 \times 14\text{mm}$  circuit area on a  $21 \times 21\text{mm}$  IC wafer. The fine line (nominally  $1\mu\text{m}$ ) measurements were made at a magnification of 2000X utilizing an optical microscope equipped with an image enhancement TV system. The lengths were measured with use a calibrated digital readout corresponding to a cursor line position on a TV screen, with a



repeatability of 5% and an estimated absolute accuracy of 20%. The results of these measurements on 132 points are presented in the histogram of Fig. 3.2-3. The standard deviation is  $0.15\mu\text{m}$ . The average gate length of one micron and the low standard deviation meet the goals of developing a manufacturable planar GaAs IC process. Linewidth measurements will be made periodically in order to establish a data base for the 4X projection lithography capability. Certainly, these data are very encouraging.

The extension of our present PMA 4-step and repeat procedure using a  $21\times 21\text{mm}$  GaAs wafer to a 9-step procedure requiring a  $30\times 30\text{mm}$  wafer has undergone initial evaluation. These larger wafers would contain  $2\frac{1}{4}$  times the circuit area of the current 6-step procedure. The main problem associated with using larger GaAs wafers is maintaining the  $\pm 1.5\mu\text{m}$  flatness tolerance required for the PMA across an entire  $30\times 30\text{mm}$  slice of GaAs, particularly during critical processes like post-implantation annealing. Before committing to the larger wafer size, some initial experiments are appropriate. The first is to take a slice of GaAs cut to the larger  $30\times 30\text{mm}$  size and evaluate its initial flatness. The flatness of both the present and larger GaAs IC wafers is shown in Fig. 3.2-4. These photographs are taken using optical interference of  $5461\text{\AA}$  Hg light between the wafer and an optical flat. These measurements were taken on cut slices before any processing had taken place. The smaller wafer (currently the standard size) has excellent flatness across the slice within the  $\pm 1.5\mu\text{m}$  flatness specification. However, the larger wafer is not as flat as the smaller wafer. The ultimate test of whether the flatness of this slice is sufficient is to actually process photolithographic patterns using the PMA. This was done using a Schottky gate-first level



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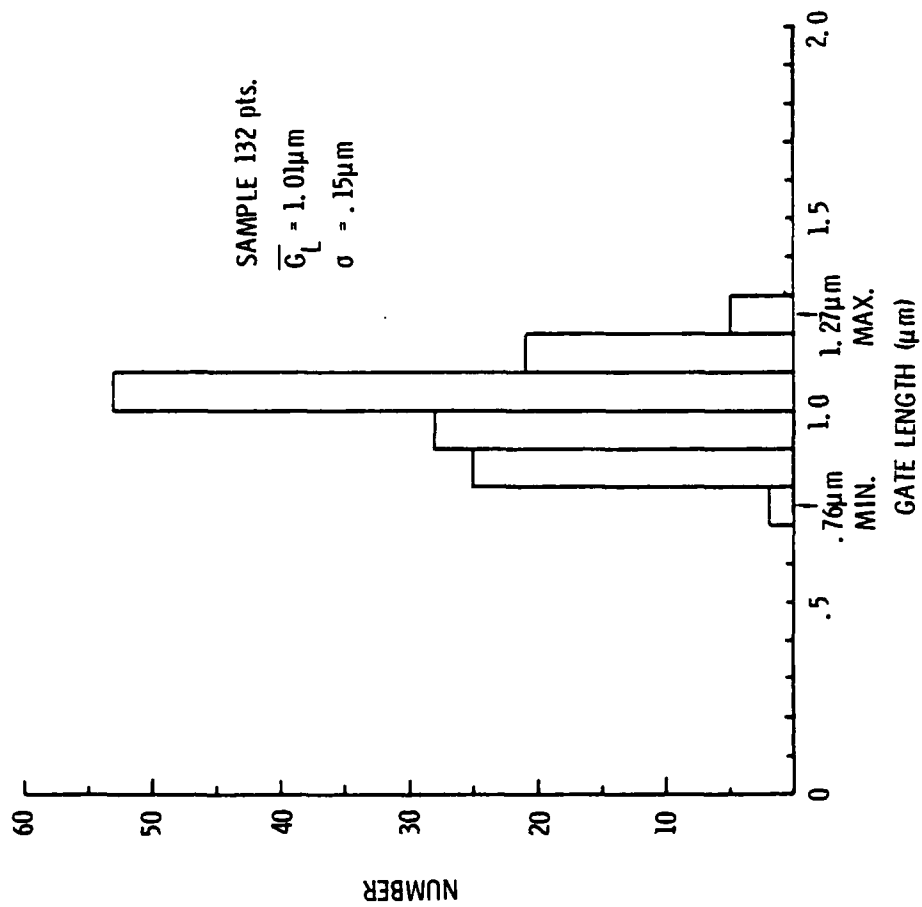


Fig. 3.2-3 Histogram showing the measured  $1\mu\text{m}$  gate length statistical distribution of 132 gates across a completed GaAs IC wafer.



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21 x 21 mm GaAs WAFER



30 x 30 mm GaAs WAFER

Fig. 3.2-4 Flatness profiles of a large GaAs wafer compared to the standard smaller wafer using an interferometric optical flat method.



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interconnect mask to expose and develop a 9-step photoresist pattern on this 30x30mm wafer. Figure 3.2-5 is a photograph of such photoresist patterns on the larger wafer shown in contrast to the same patterns on a standard wafer. The conclusion from this initial experiment is that the  $1\mu\text{m}$  features are adequately developed across the entire slice. This means that the large wafers of GaAs are processable using the 4X PMA. Experiments will be continuing on simulating the IC processes using dielectrics and annealing steps in order to determine to what extent fabrication process will affect the flatness of these wafers. If the additional experiments prove successful, full processing of larger wafers will be attempted.

### 3.2.3 Plasma Nitride

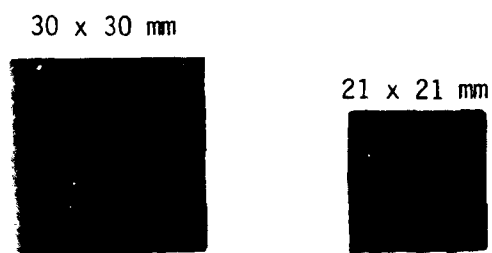
A suitable dielectric layer to serve as insulation between first and second level metalizations is an important requirement of GaAs integrated circuits. Requirements on this layer include low stress and good adherence to metals, GaAs and other dielectrics. The deposition process must be characterized by the absence of any thermal or electrical damage which might affect device parameters. Additional requirements on the dielectric include ease of etching during formation of via holes, and resistance to diffusion of potentially harmful atomic species (e.g. alkali metal ions).

Several options exist, chemical vapor deposited films of silicon dioxide or nitride, sputtered oxides or nitrides, and plasma deposited oxides or nitrides. Currently, most of the desired features are provided by plasma deposited nitride. Good adhesion, low stress, and perhaps most important, no significant shift of device parameters have been demonstrated (see Quarterly





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SCALE: 1 div = 1 mm

Fig. 3.2-5 Photograph of a large GaAs wafer exposed and developed with a 9-step PMA field compared with the 4-step PMA field on standard smaller wafer.



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Report No. 2). Plasma  $\text{Si}_3\text{N}_4$  is easy to plasma etch and it offers good resistance to diffusion of alkali ions. Deposition temperatures are compatible with GaAs ICs.

Plasma  $\text{Si}_3\text{N}_4$  films used in this program to date have been deposited using a commercial plasma deposition system, model PND301 (LFE Corp.) Initial work was done using a demonstration unit at the LFE facility in Sunnyvale, California. During this reporting period, a system was purchased and installed at the Science Center. The first step with such a new system is to duplicate previous results because films deposited in such systems are often system dependent. Such parameters as substrate temperature and system pressure are relatively easily reproduced in separate deposition systems. However, parameters such as net pumping speed and reactant residence time may be more difficult to reproduce in separate systems. The Science Center system has reproduced the deposition rates and index of refraction of the films grown in the demonstration system. The only significant difference in these films appears to be oxygen content. The oxygen content, as measured by Rutherford backscattering at the Science Center, of LFE films was 8 atomic %. Films produced in the new system at the Science Center have 4 atomic % oxygen. This is likely due to the thorough leak detection work done on the new system during installation. The 4% figure is quite respectable for a solely mechanically pumped system.

In summary, the progress in this quarter consisted of establishment of capability for deposition of plasma  $\text{Si}_3\text{N}_4$ , the film most suitable for



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the dielectric layer between first and second metalizations on GaAs ICs. The capability provides not only significantly greater convenience in processing, but also allows for further optimization of these films.



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#### 4.0 CIRCUIT MONITORING AND TESTING

Recent progress on the automation of low frequency device tests will be discussed in Sec. 4.1. Measurements of the characteristics of test devices and circuits as functions of operating temperature will be presented in Sec. 4.2. Such measurements show very promising results in the 25-133°C range. Finally, in Sec. 4.3, a simple analytical model of GaAs MESFETs suitable for circuit analysis will be discussed.

##### 4.1 Automatic Measurement System (Science Center)

The need for characterizing a large number of wafers, by performing several process monitor measurements per wafer make it mandatory to have an automatic measurement system. The system should be able to automatically step over a wafer probing the key devices (diodes and FETs) and some simple circuits (logic inverters and gates), to acquire their low frequency electrical characteristics, to analyze them, and, finally, to present the results in the form of tables, maps and histograms of key device parameters for each wafer. An automatic measurement system with such capability, capitalized with Rockwell funds, is at an advanced stage of development.

A brief description of the system was presented in the first quarterly report. As indicated in the block diagram reproduced here from that report (Fig. 4.1-1), the system makes use of an Electroglass Model 1034X automatic prober controlled by an Eclipse, Data General minicomputer. The computer, with a multiuser operating system, has 120K words of memory, and it is equipped with four discs, a magnetic tape unit and a matrix printer capable



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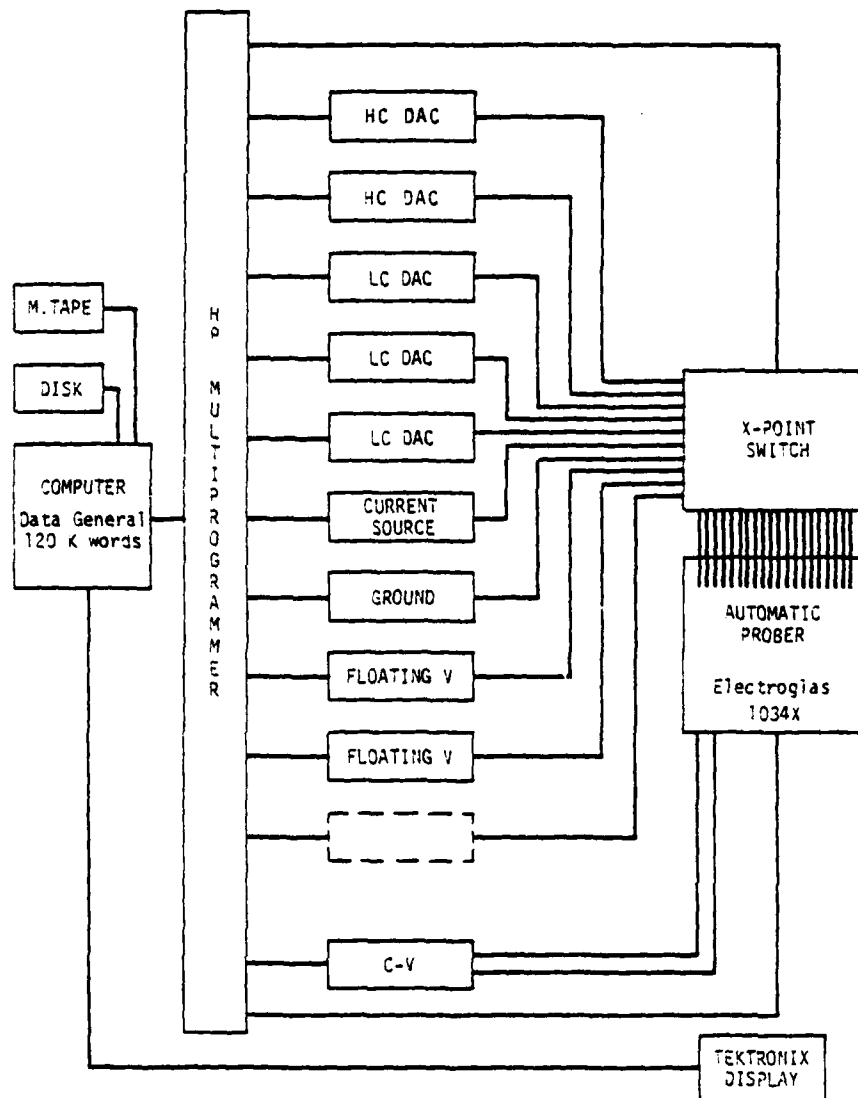


Fig. 4.1-1 Block diagram of the automatic data acquisition frequency for low frequency device characterization.



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of excellent graphic reproduction. The prober operator interfaces with the computer through a dedicated terminal with graphics capability. The heart of the data acquisition system is a set of five "digital curve tracers" (labeled DACs in Fig. 4.1-1). Each of these measurement units is capable of applying a programmed voltage to a probe and measuring the corresponding current (through 8 computer selected current ranges) performing an A/D conversion of the measured current values. In addition to the five DACs, the system has a unit for measuring floating voltages, and a programmable current source. A cross-point switch will automatically connect the probes from the probe card to the appropriate measurement units.

With the exception of the current source and the cross-point matrix, which are not essential, the system has been built, and the hardware has been made fully operational. All the software required to control the automatic prober and to operate the measurement units has been developed and tested. Fig. 4.1-2 shows, as an example, the forward I-V characteristic of a logic diode ( $1\mu\text{m} \times 2\mu\text{m}$  area). Note that the system had to step several current ranges in order to acquire the data. The result of fitting the experimental I-V characteristic is also shown, by the solid curve, in Fig. 4.1-2. The fitting parameters, namely reverse current, the ideality factor, and the series resistance (responsible for the deviation from an ideal characteristic at high current) are printed on the top of the graph.

In addition to the software required for the operation of the prober and the measurement units, a software package aimed at organizing the test programs and the data files has been developed. This software package which constitutes a "mini operating system", takes care of all the operations common



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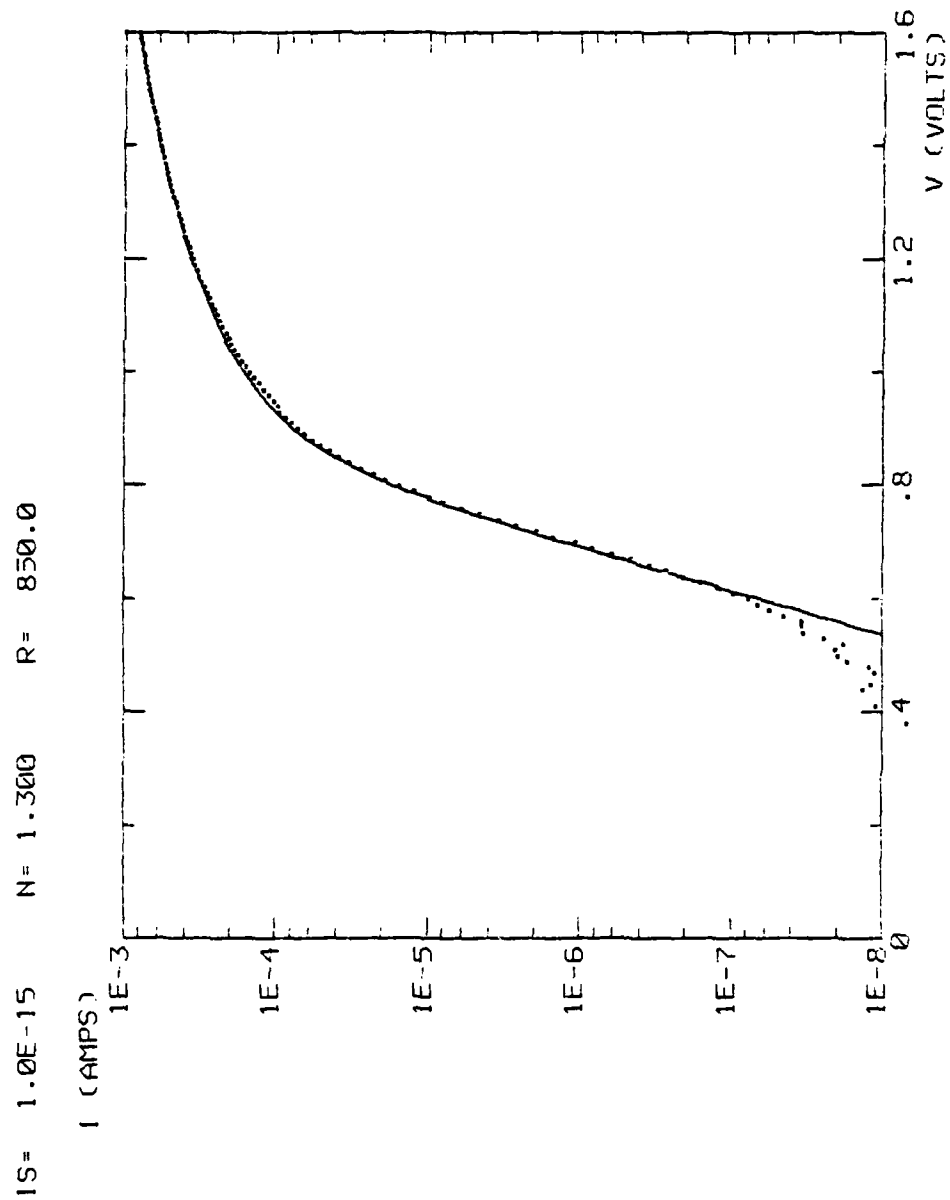


Fig. 4.1-2 Forward I-V characteristic of a logic diode ( $1\mu\text{m} \times 2\mu\text{m}$ ) recorded by the automatic measurement system. The solid line is a fit of the data. The fitting parameters are on top of the graph.



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to all the tests. This simplifies the task of the programmer who needs to write only the program features that are unique for each particular test.

At the end of this reporting period, the programs for acquisition and analysis of FET data were under development. It is expected that the system will be in full use in a very short period of time.

#### 4.2 FET Design (Science Center)

In the previous quarterly report, the characteristics of a key device in this technology, the Schottky barrier FET were discussed. By making use of a test designed in the currently used mask, the linear scaling of saturation current with channel width was investigated, showing that it could be effectively used down to  $1\mu\text{m}$  wide channels. In this reporting period the investigation of design features of the FET was continued by studying the effect of the length of the channel on the device characteristics. The results reported here were obtained from lot PD53 in the process development chip (see Fig. 4.4-2, p. 51, Quarterly Report No. 1). This lot contains several  $1\mu\text{m}$  gate FETs, all with a  $40\mu\text{m}$  wide channel, which differ from one another only by their channel length and by the magnitude of the overlapping of the edges of the layers forming the source and drain ohmic contacts.

In Fig. 4.2-1, three design configurations are shown side by side with the corresponding I-V characteristics of the devices. All three characteristics were measured on the same chip, and they were checked for reproducibility of the results over several chips on the wafer. The diagrams in Fig. 4.2-1 show that the ohmic contact metal at source and drain has been kept at the same distance ( $1.5\mu\text{m}$ ), from the edge of the gate in all three

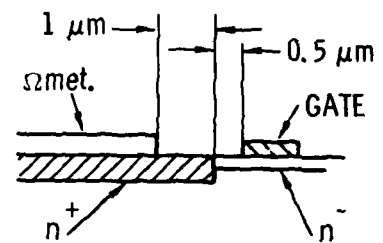




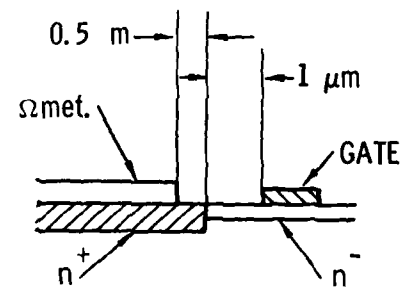
FET IN PD 53

$W = 40 \mu\text{m}$   $L_g = 1 \mu\text{m}$

1mA/div  
0.5V/div  
0.2V/step



1mA/div  
0.5V/div  
0.2V/step



2mA/div  
0.5V/div  
1V/step

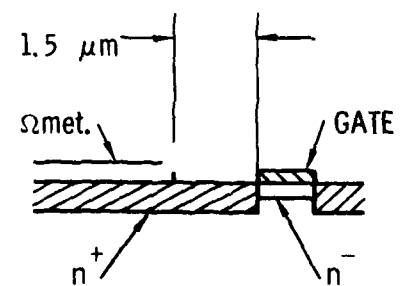


Fig. 4.2-1 Effect of source and drain design configuration on the I-V characteristics of a planar FET.



cases. The difference lies in the position of the edge of the  $n^+$  implant. The top figure corresponds to the configuration more widely used in the circuits, with  $0.5\mu\text{m}$  nominal separation between the edge of the  $n^+$  implant and the edge of the gate. The center figure corresponds to a configuration where the edge of the  $n^+$  implant has been moved away from the edge of the gate, leaving a  $1\mu\text{m}$  gap which allows for a very comfortable alignment tolerance. However, the effect of this longer channel on the I-V characteristic is an appreciable reduction of the saturation current and a slight increase of the saturation voltage. These effects are attributed to the series resistance introduced by the longer channel, which increases the effective negative voltage difference between the gate and the channel causing appreciable reduction of saturation current. Note that this reduction takes place at the expense of lowering the transconductance because the pinchoff voltage remains virtually unchanged.

By comparing the top two figures, one concludes that it is indeed beneficial to leave the channel as short as possible. The design configuration of the top figure is nearly ideal. A further reduction of nominal channel length, as shown in the bottom case of Fig. 4.2-1, is not acceptable because it causes a catastrophic increase of the saturation current and the pinchoff voltage. This is attributed to the diffusion "tails" of the  $n^+$  implant, sulfur in this case, which probably merge under the gate causing an unacceptable increase of depth and carrier concentration in the channel. The test devices in lot PD53 will be further used for the evaluation of the  $n^{++}$  ohmic contact implant when it is implemented.



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#### 4.3 Temperature Dependence of IC Operation (Science Center)

Since operation of GaAs ICs above room temperature will ultimately be required, measurements of isolation, FET I-V characteristics and SDFL NOR gate transfer characteristics have been made over the range of 25 to 133°C. In addition, to assess the effect of elevated temperature on the operating speed of gate structures, ring oscillators have also been evaluated up to 100°C. Elevated heat sink temperatures were achieved on the high speed probe station using a small hot plate fabricated from a 25 mil alumina substrate. This thin plate was located upon the normal vacuum chuck of the probe station, separated by small stand-off insulators.

In circuits with potentially high packing density, such as SDFL, adequate isolation between adjacent regions, interconnections and devices is essential to prevent the occurrence of logic errors and circuit malfunctions. To evaluate the degree to which this isolation affects or may potentially affect areas separated by very small gaps, the T1 test pattern was chosen as shown in Fig. 4.3-1. Here, a series of ohmic contacts on heavily  $n^+$  implanted GaAs are separated by 2, 3 and 5  $\mu\text{m}$  gaps of unimplanted, semi-insulating GaAs. While measurements were made on all gaps, the 3  $\mu\text{m}$  gap was selected as being representative of the minimum line separations which might be encountered in a densely packed circuit. The width of these regions is 50  $\mu\text{m}$ . Four of these test patterns are located in every PM and PD chip (see the first quarterly report for mask set organization).

Two wafers were selected for evaluation of isolation. Both integrated circuits were fabricated on substrate material which has been supplied as a contract deliverable item (ingot #3396 and #3475). Currents

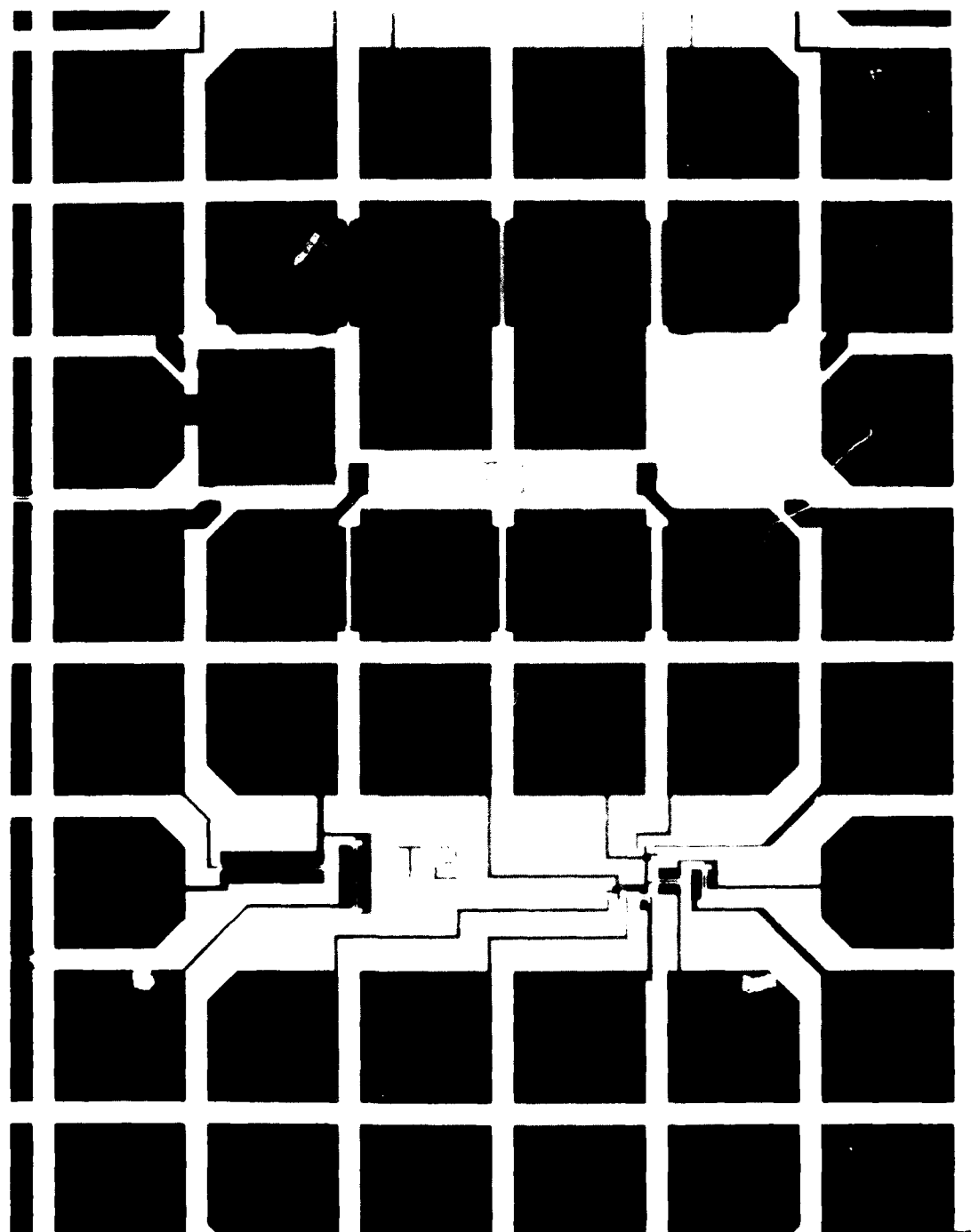


Fig. 4.3-1 Test patterns utilized for measurement of temperature dependence of isolation (T1), FET I-V characteristics and NOR gate characteristics (T2).



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between the contacts was measured up to approximately 5 volts of bias from room temperature to 133°C. The samples were biased through probes, and currents were measured with a Tektronix 577 curve tracer which is capable of resolving 1nA currents.

The results of the measurements on one wafer are presented in Fig. 4.3-2. At the top of the plot, the  $I_{DSS}$  of a  $1\mu\text{m} \times 50\mu\text{m}$  FET is shown as a reference. It is important to observe the relative magnitudes of the substrate leakage current and the  $I_{DS}$  of a FET of comparable channel dimensions. Even at the highest temperature measured, leakage was over three orders of magnitude less than normal circuit currents. Normal worst case circuit potential differences would be approximately 3 V. At this voltage level, substrate sheet resistivities can be calculated if an ohmic I-V characteristic is assumed. For this wafer, resistivities of  $2.5 \times 10^{10} \Omega/\square$  at 23°C and  $2.5 \times 10^7 \Omega/\square$  at 133°C were observed. The sheet resistivity at the maximum temperature exceeded the minimum requirement of  $10^7 \Omega/\square$  utilized for substrate selection. In addition, this was measured on wafers which had completed all of the implantations, annealing, alloying and deposition processes required for circuit fabrication. Sheet resistivities measured on the other wafer were  $8 \times 10^9 \Omega/\square$  at 23°C and  $3.3 \times 10^7 \Omega/\square$  at 105°C.

Drain current as a function of  $V_{DS}$  and  $V_{GS}$  was also measured over the same temperature range for a  $1\mu\text{m} \times 50\mu\text{m}$  FET located in test cell T2 (see Fig. 4.3-1). The  $I_{DS}$  vs  $V_{GS}$  characteristic was measured with a constant  $V_{DS} = 2.5$  V. The results of this measurement are presented in Fig. 4.3-3. The approximate 8% reduction in drain current which was observed at the highest temperature is expected from the decrease in mobility and electron



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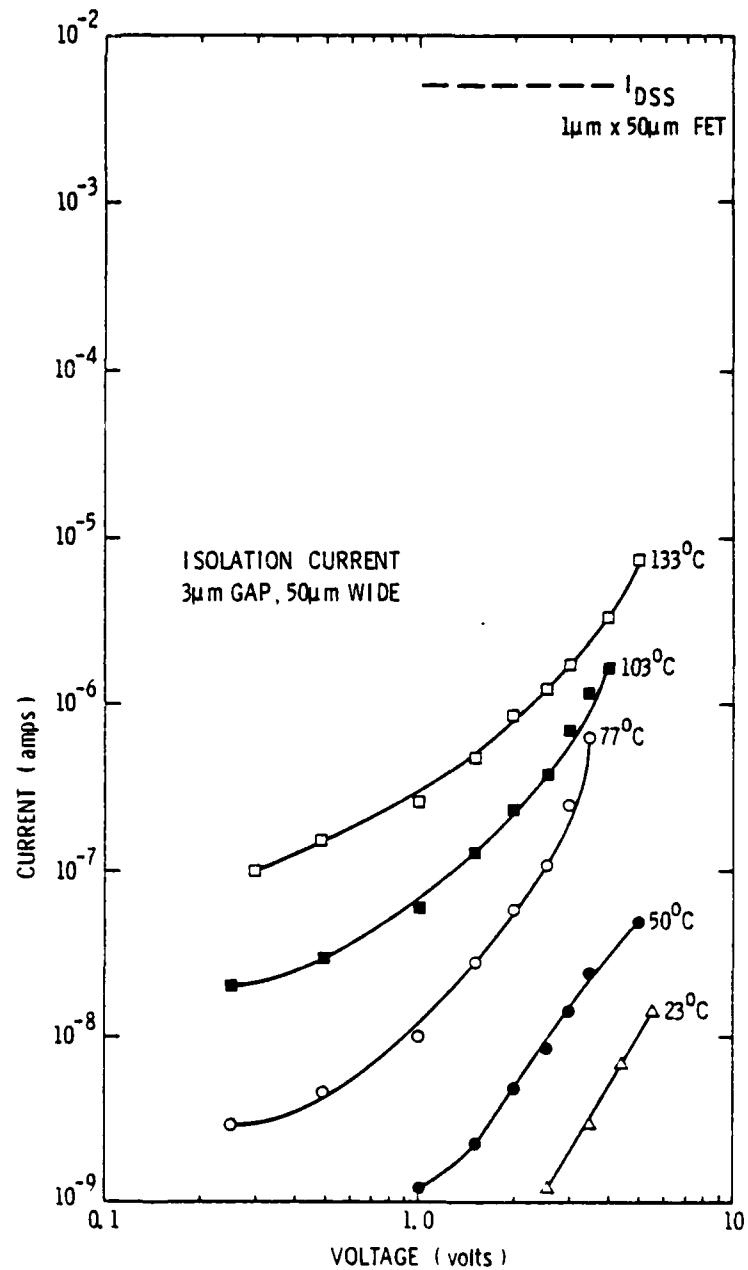


Fig. 4.3-2 Isolation current vs. voltage characteristics measured across a 3 $\mu$ m gap in semi-insulating GaAs.

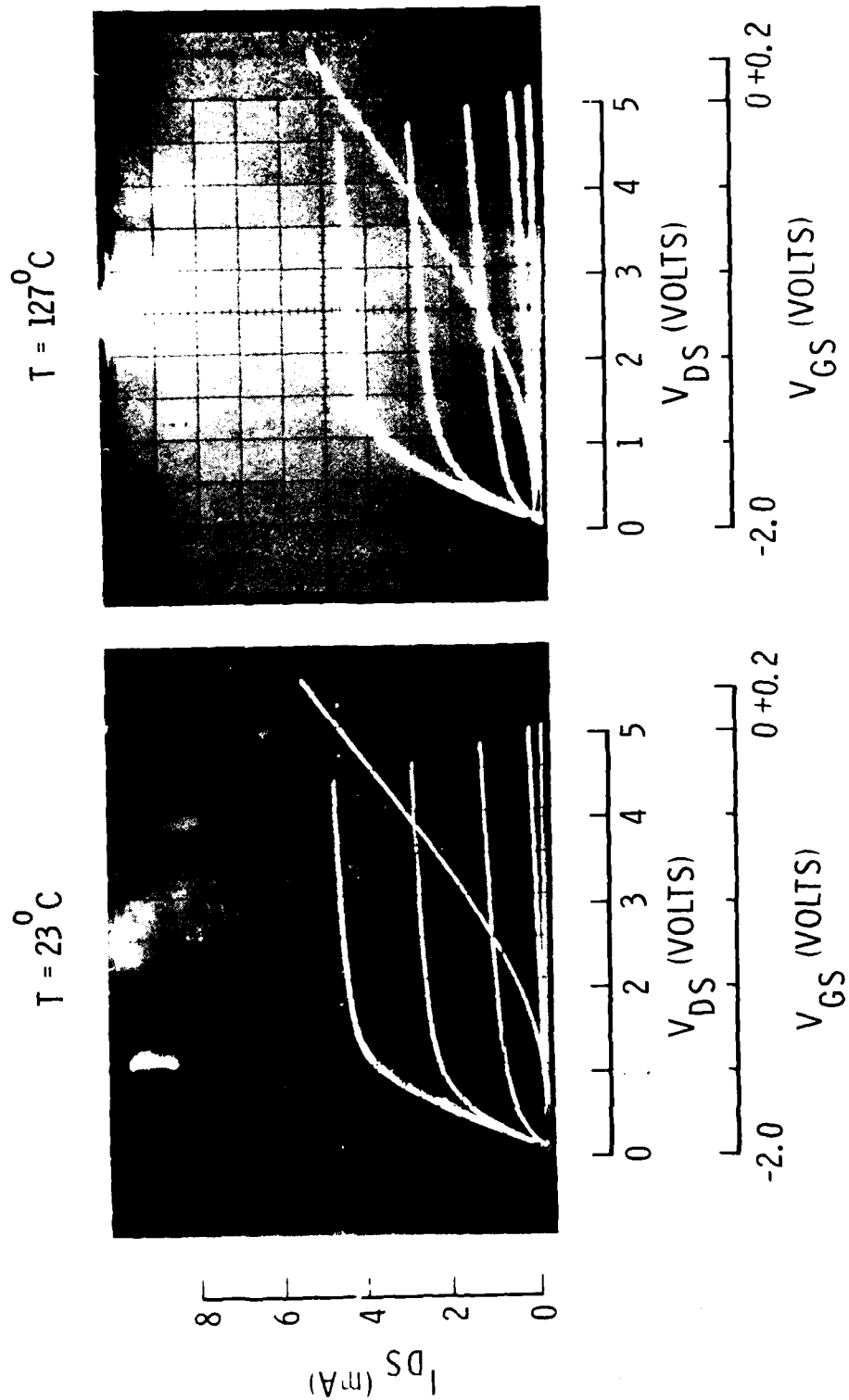


Fig. 4.3-3  $I_{DS}$  vs.  $V_{DS}$  and  $I_{DS}$  vs.  $V_{GS}$  ( $V_{DS} = 2.5$  volts) characteristics for  $1\mu\text{m} \times 50\mu\text{m}$  FET.



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drift velocity with increasing temperature. There was no change in either  $V_{DSS}$  or the pinch-off voltage of this device over the above range.

The transfer characteristics of an SDFL NOR gate should be even more sensitive to temperature since 3 FETs and 2 diodes are interconnected in the simplest case. Large shifts in the characteristics of any of the above devices would be detectable in measurements of the input vs output behavior of the gate. Therefore, measurements were made over the 23 to 103°C temperature range on a 10 $\mu$ m NOR gate located in test cell T2. This consists of a 2 input gate with level shift diode utilizing a 10 $\mu$ m inverter, 2 $\mu$ m pull-down and 7 $\mu$ m pull-up FETs. This gate is also shown in Fig. 4.3-1. A circuit diagram for this gate was shown in Section 5.1 of the second Quarterly Report.(2)

Figure 4.3-4 presents the gate output voltage,  $I_{DD}$  and  $I_{SS}$  as functions of input voltage at three operating temperatures. The supply voltages,  $V_{DD}$  and  $V_{SS}$ , were held constant. No change in the output voltage for a high or low output was observed. The threshold voltage of the gate, defined by the intersection of the transfer characteristic with the  $V_{IN} = V_{OUT}$  line, decreased slightly from 1.0 V to 0.9 V at the maximum temperature. Slight increases in  $I_{DD}$  and  $I_{SS}$  were evident as temperature was increased.

Finally, ring oscillators consisting of 9 stages of 10 $\mu$ m SDFL NOR gates were measured up to 100°C to determine the influence of temperature on the dynamic performance of a more complex circuit. These oscillators were located in subchips PD52 and PD54 and have been described in Section 5.2 of the Second Quarterly Technical Report. While fewer of these devices were





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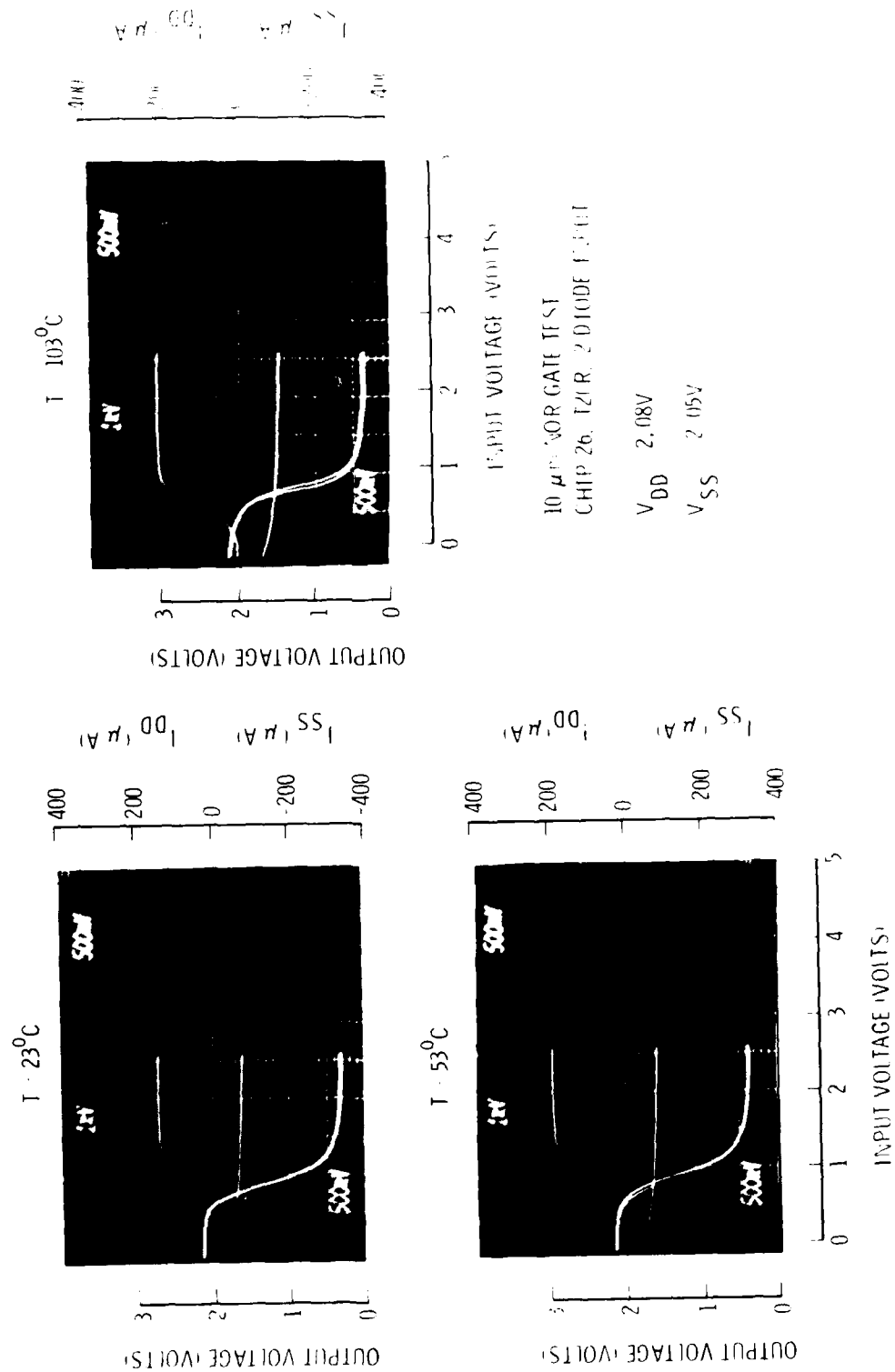


Fig. 4.3-4 Performance of 10 $\mu\text{m}$  SDFL NOR gate at three temperatures showing  $V_{out}$ ,  $I_{DD}$  and  $I_{SS}$  vs.  $V_{in}$ .



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tested than were gates or FETs, some general observations were made which were consistent among the devices evaluated. As with the discrete NOR gates, the net supply currents were observed to increase gradually with temperature. The maximum frequency of oscillation decreases slightly with temperature increase, as might be anticipated from the reduction in electron mobility and drift velocity. In one case measured, the frequency decreased from 587 MHz at room temperature ( $\tau_D = 95$  ps) to 500 MHz ( $\tau_D = 111$  ps) at 100°C. This 95 ps propagation delay result represents the fastest propagation delay reported to date on a 10 $\mu$ m SDFL ring oscillator. When the same device was biased for threshold oscillation, however, the oscillation frequency only increased from 463 MHz to 472 MHz over the same temperature range. This increase was probably due to the larger  $I_{DD}$  and  $I_{SS}$  at 100°C which results in more rapid charging of the gate, output, and parasitic capacitances.

In conclusion, initial measurements of GaAs IC device properties at elevated temperatures have yielded encouraging results. It has been demonstrated that "qualified" semi-insulating GaAs bulk substrate material maintains quite sufficient isolation to at least 133°C for FET logic circuit requirements. In addition, discrete GaAs FET and GaAs NOR gate devices have been examined and have shown quite satisfactory behavior with temperature. Finally, ring oscillators have been tested and were demonstrated to operate with performance ( $\tau_D = 111$ ps) at 100°C operating temperatures which is superior to previous results measured at room temperature.



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#### 4.4 Switching Speed Analysis (Cornell University)

In the previous quarterly report, a two-dimensional computer model of a GaAs MESFET was described, and the results of computer calculations of MESFET parameters were discussed. The model requires very short computer time while providing good agreement with experimental data and previous computer calculations. These results also provided an insight into the device physics. This insight was utilized during the last quarter to develop a new analytical model of a GaAs MESFET to get simple analytical expressions for switching times and power-delay products, and to estimate a role of the stray capacitance. Although this model is presently valid only for devices with a pinchoff voltage too high for low power logic (2-3 V vs 0.5 to 1.5 V required), it is possible to extend its validity into the low pinchoff range in order to model the performance of a full SDFL gate for ultimate integration into computer aided design of the circuits.

Experimental data, a simple theoretical consideration, a two-dimensional computer analysis, and our recent two-dimensional calculations<sup>(5)</sup> (see the previous quarterly report) show that the formation of a stationary Gunn domain at the drain side of the gate (rather than a channel pinchoff) is responsible for the current saturations in GaAs MESFETs with moderately high pinchoff voltage. If this fact is adequately taken into account, the standard Schockley theory of FETs<sup>(6)</sup> provides a very good agreement with two-dimensional computer calculations and experimental data.

The assumption made is that current saturation occurs when the average electric field under the gate reaches the domain sustaining field



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$$E_s = \frac{v_s}{\mu} \quad (1)$$

where  $v_s$  is the saturation electron drift velocity, and  $\mu$  is the low-field mobility. This assumption coupled with Shockley's theory leads to the conclusion that the saturation current  $I_{sat}$  is equal to

$$I_{sat} = g_d V_s \quad (2)$$

where

$$V_s = E_s W_G \quad (3)$$

$W_G$  is the gate length, and  $g_d$  is the drain conductance. In order to verify Eq.(2), the dependences of  $I_{sat}$  and  $g_d$  on the device thickness  $A$  were calculated in the frame of the two-dimensional model, and also compared with the results of a two-dimensional computer analysis finding good agreement.

The transconductance in the saturation region is equal to

$$g_m = \left[ \frac{q N_D \epsilon_0 \epsilon_r}{2(V_{Bi} - V_G)} \right]^{1/2} \cdot v_s \cdot W \quad (4)$$

where  $V_G$  is the gate voltage,  $W$  is the device width, and the other symbols correspond to standard notation. This result is completely different from the Shockley theory prediction according to which the transconductance in the saturation region is exactly equal to the drain conductance in the linear



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region(6). Equation (4) also agrees well with computer calculations performed in the frame of the two-dimensional model (see Fig. 4.4-1).(2)

After calculating the total charge under the gate, the following expression results for the device capacitances:

$$C_{dg} \approx C_{gs} \approx \frac{1}{2\sqrt{2}} W W_G \left( \frac{\epsilon_0 \epsilon_q N_D}{V_{Bi} - V_G} \right)^{\frac{1}{2}} \quad (5)$$

These results were also compared with the numerical calculation performed in the frame of the model previously developed(5), finding, again, good agreement between the results of the analytical and numerical calculations.

The cut-off frequency can now be calculated as

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gs}} \quad (6)$$

resulting in

$$f_T \approx \frac{1}{\pi} \frac{V_s}{W_g} \quad (7)$$

so that  $f_T \approx 25.5$  GHz for a  $1\mu\text{m}$  gate device, in good agreement with the estimates given in Ref. 4 and with our computer calculations(5).

A characteristic switching time of a GaAs MESFET can be defined as

$$\tau = \frac{Q(V_s)}{I_{sat}} \quad (8)$$



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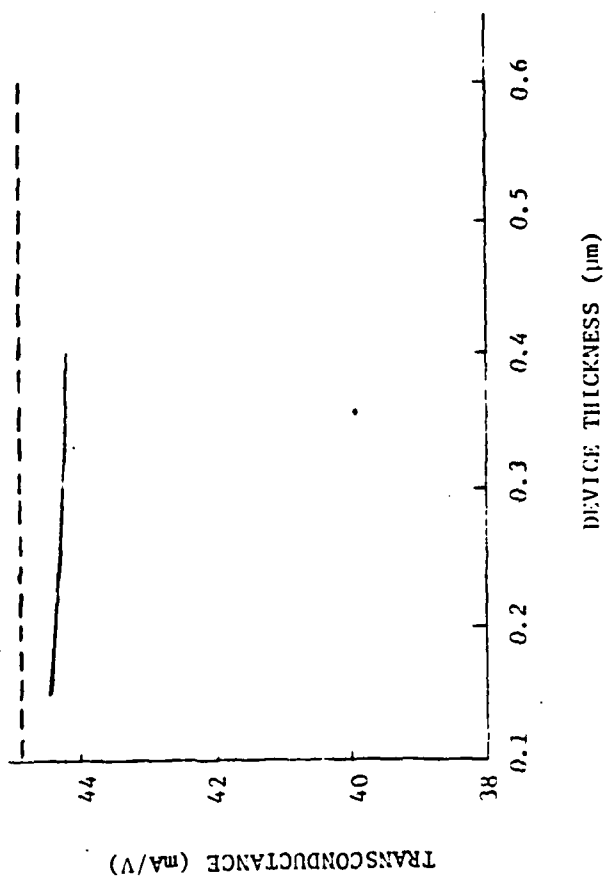


Fig. 4.4-1 Transconductance vs. device thickness for a GaAs MESFET. Dashed line: present model; solid line: computer analysis. Device parameters:  $N_D = 3 \times 10^{16} \text{ cm}^{-3}$ ,  $V_{Bi} = 0.7 \text{ V}$ ,  $A = 0.4 \mu\text{m}$ ,  $W_G = 1 \mu\text{m}$ ,  $V_S = 0.8 \times 10^7 \text{ cm/s}$ ,  $\mu = 5300 \text{ cm}^2/\text{Vs}$



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The results from this model are compared against the computer calculation in Fig. 4.4-2.

Since the switching time is proportional to the transit time under the gate, which is proportional to the saturation velocity and the gate length, it is, in principle, possible to decrease the switching time (and increase the cut-off frequency) by making the gate shorter. But there are some physical limitations on the gate length due to parasitic stray capacitance  $C_s$  between the gate, drain and source contacts. For efficient operation, it is required that

$$Q_s < Q \quad (9)$$

where  $Q$  is the charge under the gate and

$$Q_s \approx C_s (V_{Bi} - V_G) \quad (10)$$

is the stray charge. Using some estimate of stray capacitance, one can show that inequality(9) leads to the following criterion

$$W_G \geq \left[ \frac{2\epsilon_0\epsilon(V_{Bi} - V_G)}{qN_D} \right]^{1/2} \quad (11)$$

For typical parameters of a GaAs MESFET the right-hand side of Eq.(11) is about  $0.1\mu\text{m}$ . This sets an ultimate limit for a characteristic switching time in the picosecond range ( $\sim 2\text{ps}$ ).

The power required by a MESFET at the saturation point is given by



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$$P = \frac{qN_D W_G^2 A E_S}{\tau} \quad (12)$$

The power-delay product is equal to

$$P\tau \approx W W_G^2 E_S \sqrt{2\epsilon_0 \epsilon Q N_D (V_{Bi} - V_G)} \quad (13)$$

This expression has a simple physical meaning. This is the amount of work to be done in order to move the total charge of the depletion layer in the electric field  $E_S$  through the distance  $W_G$ . As shown in Fig. 4.4-3, GaAs MESFETs can yield a power delay product in the femto-joule range in good agreement with the experimental data presented in the previous quarterly report. This figure clearly demonstrates the great potential of GaAs MESFETs for high-speed, low-power integrated circuits.



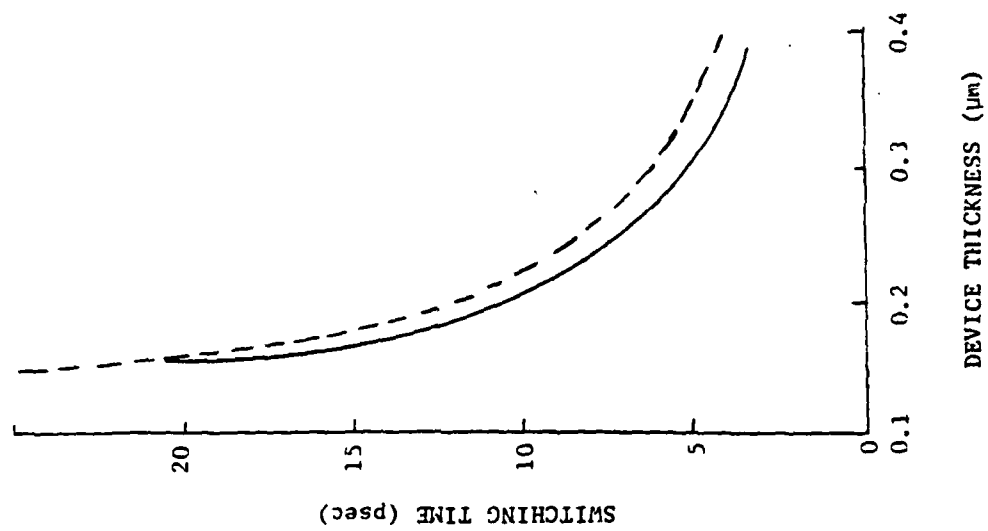


Fig. 4.4-2 Switching time vs. device thickness for a GaAs MESFET. Dashed line: analytical calculation; solid line: computer calculation. Parameters same as in Fig. 4.4-1.

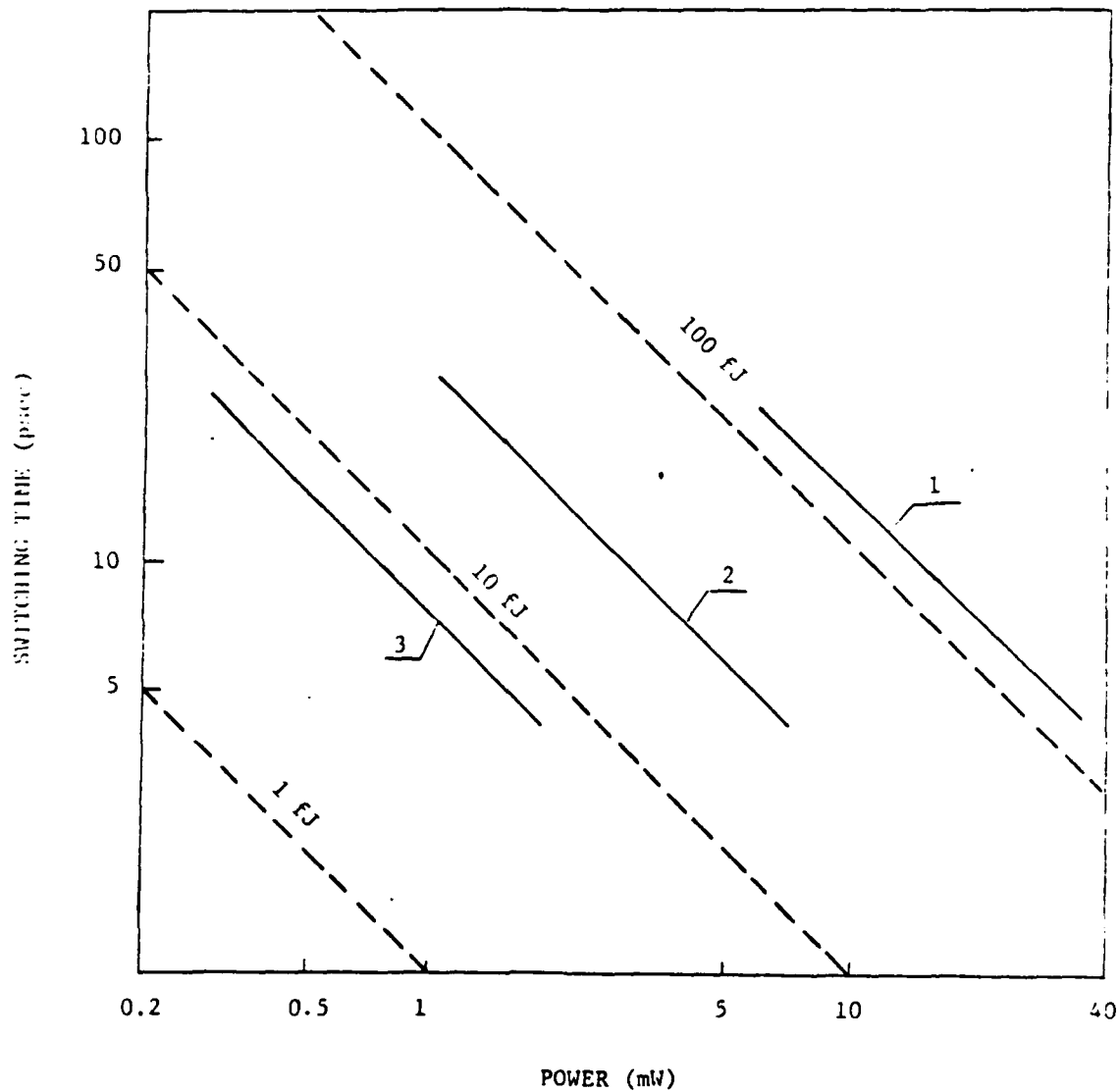


Fig. 4.4-3 Switching time vs. power for GaAs MESFETs.  
(1)  $W_G = 1 \mu m$ ,  $W = 50 \mu m$ ; (2)  $W_G = 1 \mu m$ ,  $W = 10 \mu m$ ;  
(3)  $W_G = 0.5 \mu m$ ,  $W = 10 \mu m$ .



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## 5.0 CONCLUSIONS

The implementation of all the steps required to fabricate GaAs integrated circuits and the demonstration that the expected low propagation delays and low dynamic switching energies can be achieved in these circuits, have been reported during the first two quarters of the program. The measurements of device and circuit performance as a function of operating temperature carried out during the past quarter are equal in importance to these earlier achievements. The results of these measurements indicate that the maximum operating temperature of GaAs integrated circuits should be at least as high as that of present silicon integrated circuits. In the next quarter, further measurements of performance as a function of temperature will be carried out in order to establish the maximum operating temperature for GaAs integrated circuits. In the past quarter, various process related experiments were initiated. These experiments will be guided in the future by extensive statistical data obtained using the automatic data acquisition system, which is now becoming fully operational, for measurement of device and circuit parameters. The goal of the first phase of the program is to demonstrate the capability of fabricating circuits of MSI complexity (50 to 100 gates). This represents a significant increase in complexity beyond that of the circuits such as ring oscillators fabricated to date. A new mask to be used in fabricating such circuits will be designed and fabricated during the fourth quarter of this program.



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